

Designing of a reversible fault tolerant booth multiplier

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Abstract

Conventional logic dissipates more power by losing bits of information whereas reversibility recovers bit loss from the unique input-output mapping. This paper presents the design of a reversible fault tolerant booth multiplier which can multiply both signed and unsigned numbers. The proposed circuit tolerant designed using only fault tolerant reversible gates. Thus the entire scheme inherently becomes fault tolerant. Several theorems on the numbers of gates, garbage outputs, quantum cost of the proposed design have been presented to show the efficiency of the design. The result analysis shows that the proposed design is optimized in terms of all cost parameters. The simulation of the proposed circuit verifies the correctness of the circuit.

Received: 20 August 2017

Revised: 01 January 2018

Accepted: 31 January 2018

DOI: <http://dx.doi.org/10.3329/bjisir.v53i3.38266>

Keywords: Reversible logic circuit; Fault tolerant circuit; Reversible booth multiplier; Quantum cost; Garbage output

Introduction

In recent years, the growing market of portable systems and all battery-powered electronic systems suffer from power dissipation and heat removal problem. If more and more power is dissipated, system becomes overheated and portable systems exhaust their batteries. Thus, the need of micro-electronic circuits with low power dissipation leads to the implementation of reversible logic circuit. Reversible logic gates are designed as a method to reduce the energy dissipation of logic circuit based on Landauer's concept (Landauer, 1961). According to Landauer's research, each bit of information loss dissipates at least $KT\ln 2$ joules of energy, where K is Boltzmann constant and T is the operating temperature. In room temperature T , the amount of dissipating heat is small (i.e. 2.9×10^{21} Joules), but not negligible. Bennett (Bennett, 1973) also proved that $KT\ln 2$ joules of energy dissipation will

not occur if computation is performed in a reversible manner. Among the emerging research areas, reversible logic appears to be promising due to its wide applications in recent technologies such as Quantum technology, DNA Computing, Optical Computing, CMOS, Adiabatic CMOS, Nanotechnology etc.

Multipliers are unavoidable in the design of computational units. Efficient multipliers are required for the processors to work perfectly. Multipliers work on signed and unsigned numbers. Multiplication of 2's complement numbers is a necessary operation as representation of a negative number is done using 2's complement number system and modern computers use this number system. This paper aims to design a cost efficient reversible fault tolerant Booth multiplier which can multiply both signed and unsigned numbers.

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Literature review

In this section, some important definitions regarding reversible logic is presented along with some popular reversible logic gates.

Reversible gate

A Boolean function is reversible if it maps each input assignment into a unique output assignment (Babu *et al.*, 2014). Thus, an $n \times n$ reversible logic gate can be represented as $I_v \leftrightarrow O_v$, where, $I_v = (I_1, I_2, I_3, \dots, I_{n-1}, I_n)$ is the input vector and $O_v = (O_1, O_2, O_3, \dots, O_{n-1}, O_n)$ is the output vector.

Constant inputs

The inputs that are added to an $n \times k$ function to make it reversible are called constant inputs.

Garbage outputs

Unwanted or unused outputs of a reversible gate or circuit required to maintain reversibility are known as garbage outputs (Maslov and Dueck, 2003).

Quantum cost

The quantum cost of a reversible gate (circuit) can be calculated by counting the number of elementary quantum gates required to realize the reversible function (Nielsen and Chuang, 2011). The quantum gates are inherently reversible and manipulates qubits. The most used elementary quantum gates are NOT gate (a single qubit is inverted), the Controlled-NOT (CNOT) gate (the target qubit is inverted if the control qubit is 1), the Controlled-V gate (also known as a squareroot of NOT), and the Controlled-V+ gate (Nielsen and Chuang, 2011) (performs the inverse operation of Controlled-V gate and thus is also a square root of NOT).

Delay

According to (Mohammadi and Eshghi, 2009), the delay of any 3×3 reversible gate can be computed by calculating its logical depth when it is designed from smaller 1×1 and 2×2 reversible gates with unit delay. It is denoted by Δ . For example, the Fredkin gate requires 5Δ delay.

Fault tolerant gate

The reversible gate is fault tolerant if it has one to one

mapping and if $I = (I_0 \oplus I_1 \oplus I_2 \oplus \dots \oplus I_n)$ for input and $O = (O_0 \oplus O_1 \oplus O_2 \oplus \dots \oplus O_n)$ is for output then $I = O$ (Parhami, 2006).

MIG gate

MIG gate (Islam *et al.*, 2009) is a 4×4 reversible fault tolerant gate that maps four inputs (A, B, C, D) to four outputs ($A, A \oplus B, AB \oplus C, AB' \oplus D$). The quantum cost of MIG gate is 7 and the delay is 7Δ , respectively.

LMH gate

LMH gate (Jamal *et al.*, 2013) is a 4×4 reversible fault tolerant gate that maps four inputs (A, B, C, D) to four outputs ($A, B \oplus C, A'C \oplus AB, A'C \oplus AB \oplus D$). The quantum cost and delay of LMH gate is 6 and 6Δ , respectively.

F2G Gate

F2G gate (Feynman, 1985) is a 3×3 reversible fault tolerant gate which requires three inputs (A, B, C) and three outputs ($A, A \oplus B, A \oplus C$). The quantum cost of this gate is 2 and the delay is 2Δ , respectively.

Materials and method

In this section, we present our proposed reversible fault tolerant booth multiplier. The proposed Booth's multiplier is capable of multiplying both signed and unsigned numbers. There are three components of the proposed design. First component is a reversible multi-function cell which is capable of addition, subtraction and no operation (or skip). According to the convention, this cell is called B cell. Second component is a control cell named as C cell. This cell generates two control lines such as H and D (Hayes, 1998) which are responsible for selecting various functions of B cell. We have proposed another cell named B' cell which is responsible for the addition operation in B cell.

Proposed design of reversible fault tolerant C cell

The C cell generates the control signals of array multiplier. C cell takes two inputs (X_i, X_{i-1}) that are two adjacent bits of multiplier operand. The outputs of the C cell are required two control signal named as H and D (Hayes, 1998). The C cell is implemented by reversible fault tolerant 4×4 MIG gate as shown in Fig. 1. The third and fourth input of reversible MIG

gate are set to constant zero. The proposed design reversible C cell produces two garbage outputs and requires quantum

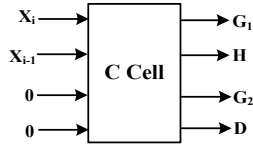


Fig. 1. Block diagram of proposed C cell

cost of 7. Since, reversible MIG gate is a fault tolerant gate, our proposed design of reversible C cell can be considered as fault tolerant.

Proposed Design of Reversible Fault Tolerant B Cell

The B cell is a multiplication cell which performs various functions include addition, subtraction and skip (no operation). These functions are defined by following equations:

$$Z = a \oplus H(b \oplus c)$$

$$C_{out} = (a \oplus D)(b \oplus c) \oplus bc$$

Here Z is the result of addition and subtraction and C_{out} indicates carry output. The cell operates on three operands a, b, c where a is the propagated result from a previous B cell, b is a multiplicand bit and c is the carry in bit. H and D is control signal generated by the corresponding C cell. When HD = 10, these equations reduce to the usual full adder

$$sum = a \oplus b \oplus c$$

$$C_{out} = ab \oplus c(a \oplus b)$$

When HD = 11, these equations reduce to the usual full adder equations:

$$sum = a \oplus b \oplus c$$

$$C_{out} = \bar{a}b \oplus \bar{a}c \oplus bc$$

equations:

When H=0, Z = a (no operation).

The block diagram of B cell is shown in Fig. 2. Proposed

reversible B cell is designed using one MIG gate, two F2G gates and two LMH gates. MIGgate takes inputs (b, c, 0,

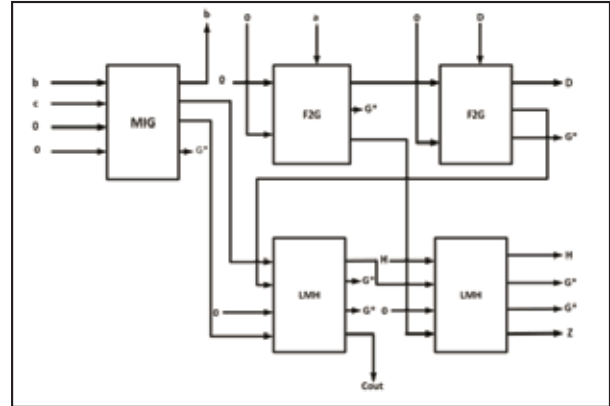


Fig. 2. Block diagram of proposed B Cell

0) and generates outputs as (b, b⊕c, bc, G*). First F2G gate takes inputs (a, 0, 0) and generates outputs as (a, G*, a). Second F2G gate takes inputs (D, a, 0) and generates outputs as (D, a⊕D, G*). First LMH gate takes inputs as (b⊕c, a⊕D, 0, bc) and generates outputs as (b⊕c, G*, G*, (b⊕c)(a⊕D) ⊕ bc). Second LMH gate takes inputs (H, b⊕c, 0, a) and generates outputs as (H, G*, G*, H(b⊕c) ⊕ a).

Proposed Design of Reversible Fault Tolerant B' Cell

Our proposed reversible B' cell is a modified B cell. It is implemented by two one F2G gate and one LMH gate. It generates one output Z. This cell used for decreasing the cost of whole circuit. In every row of our proposed Booth's multiplier the last cell is B' cell. We can used here B cell. But if we used B' cell instead of B cell the cost will be decreased. The difference between B cell and B' is B cell generates 5 outputs as (b, H, D, Z, C_{out}) and B' cell generates one output that is sum (Z). As in every row in Booth's multiplier circuit the last cell is needed to generate only sum (Z). So, if we use B' cell instead of B cell it will be better. The block diagram of B' cell is shown in Fig. 3.

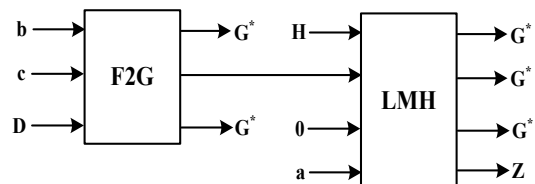


Fig. 3. Block diagram of proposed B' Cell

Proposed Design of Reversible Fault Tolerant nXn Booth Multiplier

In this paper, Booth’s multiplication method is used to find the product of signed or unsigned numbers. Our proposed reversible fault tolerant n×n booth multiplier uses n number of C cells, 2n-1 number of B cells, n number of B’ cells and additional (n-1) number of F2G gates. The proposed design is illustrated in Fig. 4.

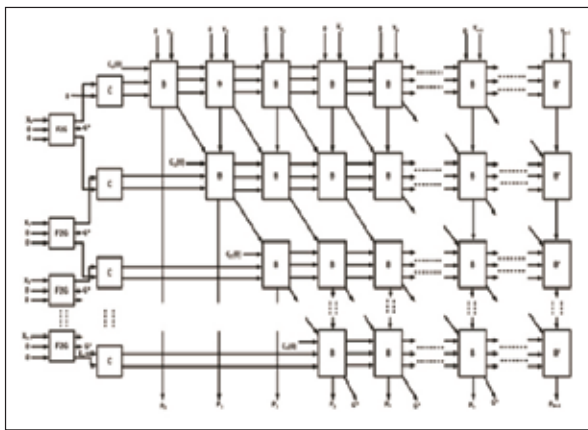


Fig. 4. Block diagram of proposed n×n reversible fault tolerant booth multiplier

According to Fig. 4, X is the multiplier and Y is the multiplicand of our proposed n×n reversible Booth’s multiplier. In the first step, each bit of the multiplier X_i (i = 0, 1, ..., n-1) is fed to a F2G gate which is responsible for copying the corresponding bit of the multiplier X.

Secondly, the outputs of F2G gates are fed to our proposed reversible C cell. Each C cell in the ith (i = 0, 1, ..., n-1) row takes two bits X_{i-1} and X_i of the multiplier as inputs except the C cell in the first row which takes X₀ and constant 0 as inputs.

Each B cell takes bits from the multiplicand Y_i (i = 0, 1, ..., n-1). The first B cell of each row takes constant 0 as carry input. Rest of the B cells takes C_{out} of the previous B cell in the same row. Besides, each B or B’ cell takes two control input H and D, produced by C cell in the corresponding row.

In the last level, B’ cell is used that only produces output Z. Since, it takes less number of gates to construct B’ cell as shown in Fig. 3, number of gates in the whole circuit is minimized using B’ cells rather than B cells.

Theorem 1. If N_G is the total number of gates required to implement an n×n reversible fault tolerant Booth multiplier, then,

$$N_G = \frac{(15n^2 - 7n - 2)}{2} \text{ where } n \text{ is the number of bits.}$$

Proof. We prove the above statement by induction on the number of bits (n).

According to our design, the proposed 2 × 2 reversible fault tolerant Booth multiplier requires 22(= ((15 × 4) - (7 × 2) - 2) / 2) number of gates. Thus, the theorem holds for the base case (n = 2).

For n = k the number of gates N_G = (15k² - 7k - 2) / 2 is true.

For n = k + 1, the number of B cell is 3(k + 1)k, number of B’ cell is k + 1, number of C cell is k + 1, and also the number of F2G gate is k. In our proposed design, each B, B’ and C cell includes 5, 2 and 1 fault tolerant gates respectively. Thus, total number of gates,

So, if N_G is the total number of gates required to implement

$$\begin{aligned} N_G &= 5 \frac{3}{2} (k + 1)k + 2(k + 1) + k + 1 + k \\ &= \frac{(15k^2 + 23k + 6)}{2} \\ &= \frac{(15(k + 1)^2 - 7(k + 1) - 2)}{2} \end{aligned}$$

an n×n reversible fault tolerant Booth multiplier, then N_G = (15n² - 7n - 2) / 2, where n is the number of bits.

Theorem 2. If G_O is the total number of garbage outputs for n×n reversible fault tolerant booth multiplier, then G_O = (21n² - 5n - 2) / 2, where n is the no. of bits.

Proof. We prove the above statement by induction on the number of bits (n).

According to our design, 2 × 2 fault tolerant reversible Booth multiplier produces total 36(= ((21 × 4) - (5 × 2) - 2) / 2) garbage outputs. So, the theorem holds for the base case (n = 2).

We assume, for n = k the garbage output G_O = (21k² - 5k - 2) / 2.

For $n = k+1$, the number of B cell is $\frac{3}{2}(k+1)k$, number of B' cell is $k+1$, number of C cell is $k+1$ and also the number of F2G gate is k . In our proposed design each B cell, B' cell, C cell and F2G gate respectively includes 7, 5, 2 and 1 garbage outputs. Thus, total garbage outputs is,

$$\begin{aligned} G_o &= 7\frac{3}{2}(k+1)k + 5(k+1) + 2(k+1) + k \\ &= (21k^2 + 37k + 14)/2 \\ &= (21(k+1)^2 - 5(k+1) - 2)/2 \end{aligned}$$

So, if G_o is the total number of garbage outputs for $n \times n$ fault tolerant reversible Booth multiplier, then $G_o = (21n^2 - 5n - 2)/2$, where, n is the no. of bits.

Theorem 3. If Q_c be the total quantum cost of an $n \times n$ reversible fault tolerant Booth multiplier, then, $Q_c = (69n^2 - 35n - 4)/2$ where n is the number of bits.

Proof. We prove the above statement by induction on the number of bits (n).

For $n = 2$, the quantum cost is 101 ($= ((69 \times 4) - (35 \times 2) - 4)/2$). So, the theorem holds for the base case ($n = 2$).

For $n = k$, we assume $Q_c = (69k^2 - 35k - 4)/2$ is true.

For $n = k+1$, the number of B cell is $\frac{3}{2}(k+1)k$, number of B' cell is $k+1$, number of C cell is $k+1$ and also the number of F2G gate is k . In our proposed design each B cell, B' cell, C cell and F2G gate requires 23, 8, 7 and 2 quantum cost respectively. So, total quantum cost is

$$\begin{aligned} Q_c &= 23\frac{3}{2}(k+1)k + 8(k+1) + 7(k+1) + 2k \\ &= (69k^2 + 103k + 30)/2 \\ &= (69(k+1)^2 - 35(k+1) - 4)/2 \end{aligned}$$

So, if Q_c be the total quantum cost of an $n \times n$ reversible fault tolerant Booth multiplier, then $Q_c = (69n^2 - 35n - 4)/2$, where n is the number of bits.

Results and discussion

This section analyzes different cost parameters such as number of gates, garbage outputs and quantum cost of proposed 2-bit, 4-bit, 8-bit and 16-bit reversible fault tolerant booth multipliers. According to the graph shown in Fig. 5, gate count, garbage output and quantum cost are gradually increasing as number of bits of the multiplicand and multiplier of our proposed reversible fault tolerant booth

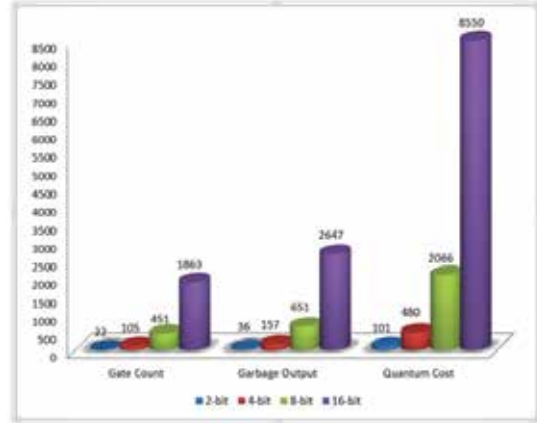


Fig. 5. Evaluation of proposed 2-bit, 4-bit, 8-bit and 16-bit reversible fault tolerant booth multipliers

Table I. Comparison of proposed 2-bit, 4-bit, 8-bit and 16-bit reversible fault tolerant booth multipliers

No. of bits	No. of gates	Garbage outputs	Quantum cost
2	22	36	101
4	105	157	480
8	451	651	2066
16	1863	2647	8550
n	$(15n^2 - 7n - 2)/2$	$(21n^2 - 5n - 2)/2$	$(69n^2 - 35n - 4)/2$

multiplier is increased. Table I summarizes the cost parameters of reversible fault tolerant booth multipliers for 2-bit, 4-bit, 8-bit, 16-bit and n -bit multiplicand and multiplier. We avoid comparing our paper with existing reversible booth's multiplier presented in (Sultana *et al.*, 2015) as the existing design is not fault tolerant. The simulation of our proposed 3×3 reversible fault tolerant booth multiplier is performed using Microwind DSCH 3.0 (DSCH, 2017) software on a computer that has Intel(R) Core (TM)i7-4790 CPU with 3.60 GHz Clock Speed and 4.00 GB RAM. Fig. 6 shows the simulation result of the proposed $3 \times$

3 reversible fault tolerant booth multiplier. Assume that the two operands are -3 and 2. Obviously the negative input will be in 2's complement form. Hence, multiplier $X = 101$ (-3 in decimal), multiplicand $Y = 010$ (positive 2 in decimal). According to the output of the simulation as shown in Fig. 6, the result is 11010 (-6 in decimal). So, the simulation result verifies the correctness of the proposed circuit.

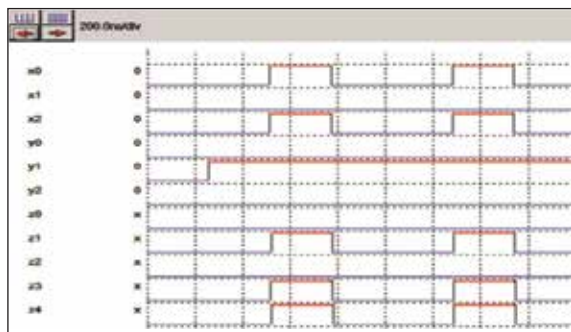


Fig. 6. Simulation of proposed 3 x 3 reversible fault tolerant booth multiplier

Conclusion

This paper presents the design architecture of reversible Booth multiplier using fault tolerant gates. As our proposed work is fault tolerant, the proposed design incurs more gates, garbage output, quantum cost and delay than the existing one but it facilitates to detect unexpected and sudden errors of different components of the circuit. Besides, the fault tolerance property also enables the circuit to continue operating properly in the event of the failure of some of its components. The proposed circuit can be implemented in reversible programmable logic arrays (Mitra *et al.*, 2012). The proposed circuit can be used in embedded processors such as, digital signal processors, high performance processors, high speed and low power applications, reversible fault tolerant arithmetic logic unit etc.

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