GUBJSE: ISSN: 2409-0476

Performance Evaluation of Cascaded and Reduced Switch Multilevel Inverter Using Modified Carrier Based PWM Technique

Md. Tariqul Islam, Md. Fayzur Rahman, A. A. Md. Monzur-Ul-Akhir and Zisun Ahmed

Abstract — This paper proposes an improved harmonic distorted modified triangular carrier-based multicarrier pulse width modulation for generating the switching pulses of a multilevel inverter. This modified triangular wave consists of a triangular wave bearing a close resemblance to an 'M' shaped wave. The design of this carrier signal has been optimized to maintain a low level of total harmonic distortion (THD), while increasing the fundamental o/p voltage to ensure the effective DC voltage utilization. Moreover, this optimization reduces the switching losses and improve the efficiency of the power inverter. With the help of this carrier signal, High-frequency alternative phase opposition disposition pulse width modulation (APODPWM) is generated. This new control scheme has been applied to seven levels of conventional cascaded H-bridge with reduced switch multilevel inverter. The output is compared with conventional carrier-based APODPWM. The comparison is made in terms of THD, fundamental output voltages and inverter losses. To ensure quality performance, conventional carrier and modified carrier-based multicarrier PWM topologies are used for the Cascaded seven-level inverter with reduced switch seven-level inverter having a carrier frequency of 2 kHz and modulation index of 0.8-1.30. According to the simulation results, by using the proposed modulation scheme the THD and the switching loss were reduced by 9.64[%] and 4.2[%] respectively. Besides, the proposed modulation technique increases the fundamental output voltages. The total simulation process is done in MATLAB Simulink environment.

This paper was received on 18 August 2020, revised on 8 September 2020 and accepted on 13 October 2020. This work was supported financially in part by the Department of EEE, GUB under Grant number 2019.

Md. Tariqul Islam is with the Electrical and Electronic Engineering Department, Green University of Bangladesh, Dhaka, Bangladesh. E-mail: *tariqul@eee.green.edu.bd.*

Md. Fayzur Rahman is with the Electrical and Electronic Engineering Department, Green University of Bangladesh, Dhaka, Bangladesh. E-mail: *drfayzur@eee.green.edu.bd.*

A. A. Md. Monzur-Ul-Akhir is with the Electrical and Electronic Engineering Department, Green University of Bangladesh, Dhaka, Bangladesh. E-mail: *monzur@eee.green.edu.bd*

Zisun Ahmed is with the Electrical and Electronic Engineering Department, Green University of Bangladesh, Dhaka, Bangladesh. E-mail: *zisun@eee.green.edu.bd.*

Index Terms — Multilevel Inverter, Total Harmonic Distortion, Modified carrier, Conventional carrier, Modulation Algorithm, Inverter loss, Level shifted topology, Cascaded seven level inverter, Reduced switch seven level inverter, MATLAB/Simulink.

I. Introduction

In recent decades, the improvement of sustainable power sources such as, solar, wind and geo-thermal energies has drawn tremendous research attention due to rapidly increasing concerns over climate change and scarcity of fossil fuel reserves. Solar radiation is among the most significant wellspring of sustainable power sources accessible today. Solar radiation is converted into electricity with the help of photovoltaic panels [1]. The output of the photovoltaic panel is DC power. For adjusting this photovoltaic output with grid and home applicants, a power inverter is needed which converts the dc power into ac power. For DC to AC voltage conversion, the first two-level inverter was proposed which had one voltage source and two power switches. This topology is suitable for low voltage applications having numerous disadvantages like high voltage stress on the switches, high total harmonic distortion, and higher switching losses [2]. To solve this problem, multilevel inverter was first proposed by Baker and Banister in 1965[3]. The idea was to create a higher voltage output in small voltage ventures by using more dc voltage and switches. The inverter approaches close to the sinusoidal output by increasing the number of voltage levels. Compared to the two-level inverter, a multilevel inverter has many advantages like low switching losses, low total harmonics distortion, reduced voltage stress across the power switches, low electromagnetic interference and lower dv/dt ratio among others [4].

The diode-clamped, flying capacitor and cascaded multilevel inverter are the basic bias [5]. The referenced structures utilize comparable quantities of switches. In any case, the quantity of on-state switches in a present way in the flying-capacitor and diode-clamped multilevel inverters is not as much as cascaded topology which diminishes the conduction

and exchanging misfortunes. Utilization of high quantities of capacitors and diodes are the fundamental hindrances of the flying capacitor and diode-clamped multilevel inverters. Likewise, adjusting the voltage of capacitors in the flying capacitor and diode-clamped multilevel inverters is another burden. The cascaded multilevel inverter utilizes an enormous number of dc voltage hotspots for delivering more elevated levels which build the circuit size and converter cost [6].

Nowadays reduced switch multilevel inverter is more commonplace in modern technology. Different types of control techniques are introduced for generating a switching pulse. The most popular switching techniques are carrier-based modulation, staircase or level control modulation, selective harmonics modulation, and space vector pulse width modulation. Furthermore, carrier-based modulation can be categorized into two distinct methods. One is reference signal modulation and another is carrier signal modulation. This carrier signal modulation is also known as multicarrier pulse width modulation [7]. Diverse Multicarrier PWM strategy has been introduced in this paper attempted to determine the ideal condition for diminishing THD impact on the output waveform of the multilevel inverter. Accordingly, to diminish the THD impact, probably the best arrangement is to embed a filter circuit in the output of an inverter however this action is exorbitant and makes the inverter cumbersome.

Subsequently, to scale down the expense and size of the filter circuit, this paper proposes a modified carrier-based multicarrier PWM method that offers less THD and expanded fundamental output voltages than regular multicarrier procedures. This new control scheme is applied to seven-level conventional cascaded H-bridge and reduced switch multilevel inverter and compared with conventional carrier-based multicarrier PWM technique. The comparison is made in terms of total harmonic distortions (THDs), fundamental output voltage and inverter loss. To ensure quality performance, level shifted conventional carrier and modified carrier based PWM topologies are used for the Cascaded seven-level inverter to yield reduced switch seven-level inverter with a carrier frequency of 2 kHz and modulation index of 0.8-1.30.

This paper has been organized as follows: section two deals with cascaded H-bridge and reduced switch multilevel inverter, section III deals with multicarrier pulse width modulation technique, section IV deals with calculation of inverter loss, section V deals with simulation results, section VI deals with performance analysis, section VII deals with comparative study and finally the article ends with conclusion and references.

II. Cascaded H-Bridge and Reduced Switch H-Bridge Inverter

The H-bridge multilevel inverter mainly is of two types. One is the cascaded H-bridge multilevel inverter and another is the reduced switch H-Bridge multilevel inverter. Fig. 1(a) shows the circuit diagram of cascaded seven-level inverter. It consists of three number of H-bridge cells. Each cell consists of four controlled semiconductor switches. IGBT is most popularly used controlling switches for inverter. Each bridge is connected in series. Each bridge can generate output voltages V_{dc} , 0, $-V_{dc}$. The output of each bridge is connected in series, that's why we get stair case output voltage across the load. A reduced switch seven-level inverter is presented in fig. 1(b). Here the voltage source magnitudes are different from each other. The operations of cascade multilevel inverter, reduced switch multilevel inverter are presented in [8] – [9]. The switching sequence of conventional H-bridge and reduce switch H-bridge are shown in table 1 and table 2 respectively.

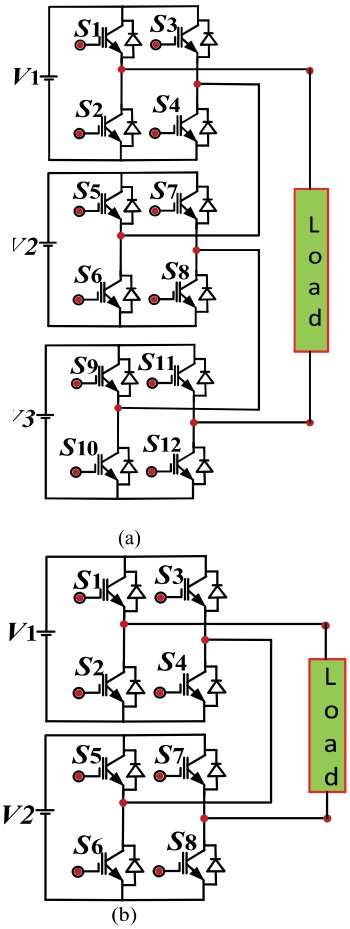


Fig. 1. Seven level inverters (a) cascaded H-bridge (b) reduced switch topology.

TABLE I
SWITCHING STATES OF CONVENTIONAL SINGLE PHASE 7-LEVEL INVERTER

State	Switching states												V_{out}
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	
1	0	1	0	1	0	1	0	1	0	1	0	0	0
2	1	0	0	1	0	1	0	1	0	1	0	0	V
3	1	0	0	1	1	0	0	1	0	1	0	1	2V
4	1	0	0	1	1	0	0	1	1	1	0	0	3V
5	0	0	0	1	0	1	0	1	1	1	0	0	-V
6	0	1	0	1	0	1	1	0	0	0	1	0	-2V
7	0	1	1	0	0	1	1	0	0	0	1	1	-3V

TABLE II
SWITCHING STATES OF SINGLE PHASE REDUCED SWITCH 7-LEVEL INVERTER

State	Switching states								V_{out}
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	
1	1	0	0	1	1	0	1	0	V_1
2	1	0	1	0	1	0	0	1	V_2
3	1	0	0	1	1	0	0	1	V_1+V_2
4	0	1	0	1	1	0	1	0	0
5	0	1	1	0	1	0	1	0	$-V_1$
6	1	0	1	0	0	1	1	0	$-V_2$
7	0	1	1	0	0	1	1	0	$-V_1-V_2$

III. CASCADED H-BRIDGE AND REDUCED SWITCH H-BRIDGE INVERTER

Multicarrier switching techniques have gained their popularity among various switching technique of power inverter because of low THD, improved power quality, increased fundamental output voltage and lower losses. In this topology, several carrier waves are used for generating switching pulse. For this reason, this topology is known as multicarrier techniques. Based on the arrangement of carriers, multicarrier technique is divided into five categories like phase disposition(PD), phase opposition disposition(POD), alternative phase opposition disposition (APOD), variable frequency (VF), Carrier overlapping (CO) [10].In phase disposition, all carrier signal are in phase with one another and in phase opposition disposition arrangement, all carrier signal are divided into two groups. Above the zero level is considered as positive carriers and below the zero level is considered as negative carriers. The phase difference between positive and negative carriers is 180 degree. Again in alternative phase opposition disposition arrangement, all carriers are out of phase with one another. All these three techniques, the carrier are same frequency and same magnitude. Variable frequency arrangement can be obtained by using different frequency of carrier signals. But in overlapping arrangement, the magnitude of different carrier signals is different.

The modulation index is calculated as

$$m_a = \frac{V_m}{(m-1)V_{cr}} \quad (1)$$

where V_{cr}= peak value of each carrier wave, m=number of level, V_m=peak value of modulating wave. The frequency modulation index can be calculated as

$$m_f = \frac{f_{cr}}{f_m} \quad (2)$$

Among these techniques, APODPWM arrangement offers better results [5]. For this reason, only APODPWM technique has been considered in this paper.

A. Conventional Triangular Signal

This triangular wave is periodic, linear and

continuous function. This signal is generated in MATLAB using conventional block in MATLAB Simulation. Fig. 2 shows the generation of conventional carrier signal for multicarrier PWM technique. Fig. 3 shows the conventional triangular wave that is frequently used as a carrier signal with modulating signal to generate pulse.

B. Modified Triangular Signal

The modified triangular carrier signal is used as carrier signal for modular multilevel inverter. It has two parts. One is triangular signal generation part and another is modified part. Fig. 4 shows the generation of modified carrier signal for multicarrier PWM technique. Fig. 5 shows a new carrier signal which is the modified version of triangular wave. It is also a periodic and continuous function of time. This modified triangular wave consists of a triangular wave along with an 'M' shape wave. This proposed wave-shape shows better performance than existing triangular wave.

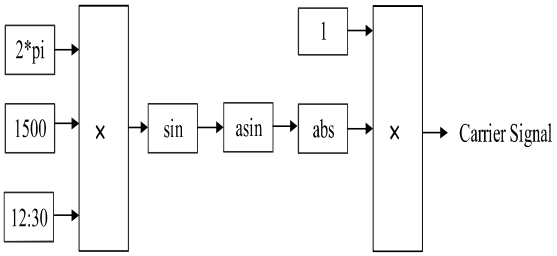


Fig. 2. Conventional carrier signal generation for multicarrier PWM technique.

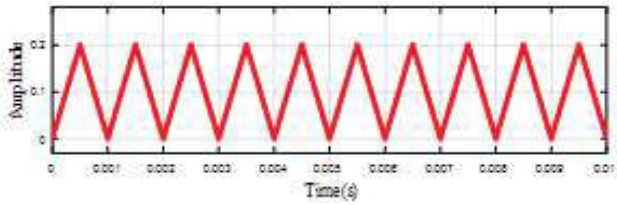


Fig. 3. Conventional triangular carrier signal.

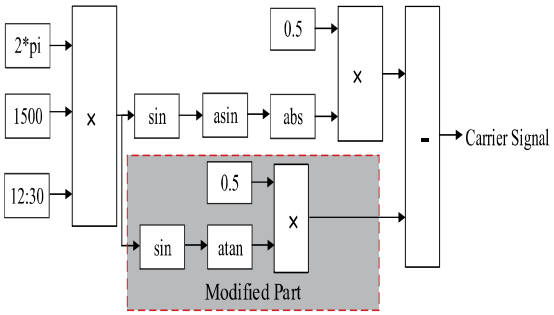


Fig. 4. Modified carrier signal generation for multicarrier PWM technique.

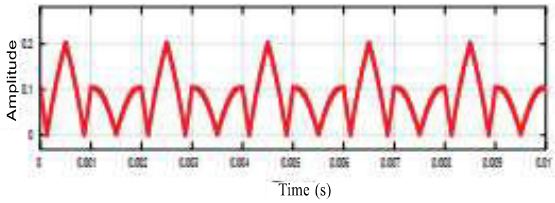
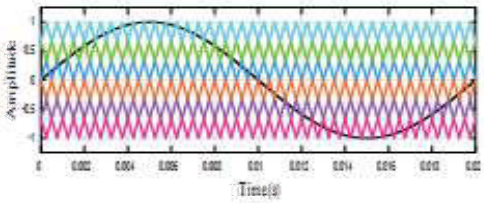
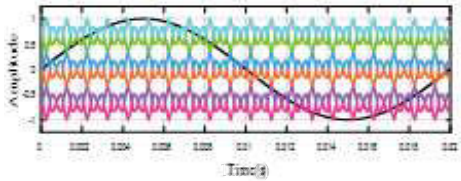


Fig. 5. Modified carrier signal for multicarrier PWM technique.

The APOD scheme for 7-level inverter is illustrated in fig. 6.



(a)



(b)

Fig. 6. APODPWM arrangement for (a) Conventional carrier (b) Modified carrier.

IV. CALCULATION OF INVERTER LOSS

Power losses play an essential role for determining the efficiency of a power inverter. Basically, the efficiency is the ratio of output power to the summation of output power plus losses. So, large power losses decrease the efficiency of a power inverter. Therefore for designing a power inverter, it is important to keep the power loss as low as possible. Mainly two types of losses such as conduction losses and power losses are introduced this inverter loss. Conduction loss which occurs when anti-parallel diode and switch carry current otherwise this loss is zero. Contrariwise the switching loss occurs due to turn on or off of switch and diode.

The computation of conduction power losses [11] can be calculated by using equation 3-5

$$P_{cond\_IGBT} = \frac{1}{2\pi}\int_{0}^{2\pi} V_{ce}(\theta) \times I(\theta) \times V_{cmd}(\theta) d\theta \quad (3)$$

$$P_{cond\_D} = \frac{1}{2\pi}\int_{0}^{2\pi} V_{F}(\theta) \times I(\theta) \times V_{cmd}(\theta) d\theta \quad (4)$$

$$P_{cond} = P_{cond\_IGBT} + P_{cond\_D} \quad (5)$$

where $I(\theta)$ is the load current, $V_{cmd}(\theta)$ is the PWM signal of the IGBT, $V_{ce}(\theta)$ is the voltage across switch, $V_F(\theta)$ is the voltage across diode.

Also, the switching loss can be calculated as

$$P_{sw} = \frac{1}{T}\sum E_{on} + E_{off} + E_{rec} \quad (6)$$

where E_{on} is the turn on commutation, E_{off} is the turn off commutation, E_{rec} is the diode reverse recovery process.

In this paper, for the loss calculation, an identical IGBT module FF150R12KT3G is considered for both switching technique Mathematical models acquired for the IGBT module FF150R12KT3G [11] are given by

$$V_{ce} = 1.15e^{0.00226I(\theta)} - 0.6654e^{-0.044I(\theta)} \quad (7)$$

$$V_F = 1.2e^{0.002I(\theta)} - 0.72584e^{-0.0475I(\theta)} \quad (8)$$

$$E_{on} = 0.0051e^{0.0064I(\theta)} - 0.0037e^{-0.00811I(\theta)} \quad (9)$$

$$E_{off} = 0.0643e^{0.00121I(\theta)} - 0.0647e^{-0.00107I(\theta)} \quad (10)$$

$$E_{rec} = 0.01806e^{0.000412I(\theta)} - 0.0157e^{-0.06736I(\theta)} \quad (11)$$

$$I(\theta) = M \times I_{max} \quad (12)$$

where $I(\theta)$ =Load current, M=modulation index, $\emptyset$ = Phase shifted between voltage and current. Here, only switching loss is considered for comparison.

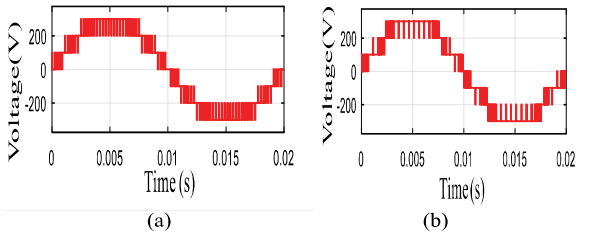
V. Simulation Result

Both conventional and modified triangular based APODPWM techniques are analyzed for seven-level cascaded and reduced switch multilevel inverter using MATLAB Simulink software. The obtained result from MATLAB Simulation will help us to verify our proposed modified triangular based multicarrier SPWM technique and also helps to prove that the proposed topology is better than the conventional one.

Fig. 7 appearances the output voltage waveform of cascaded 7-level inverter topology using modified and conventional triangular based APODPWM technique. Fig. 8 displays the output voltage waveform of reduced switch 7-level inverter topology using modified and conventional triangular based APODPWM techniques. Here the output voltages of these topologies are almost same. Differences can be observed in harmonic spectrum of these output voltages presented in fig. 9 and fig. 10 respectively.

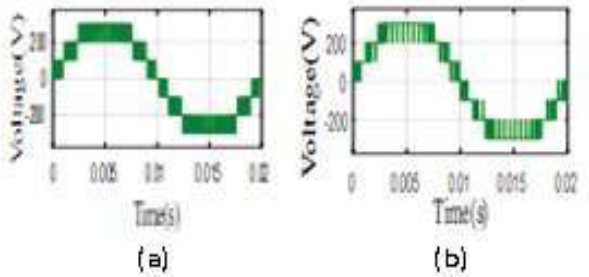
VI. Performance Analysis

The performance of both conventional and proposed modified triangular APODPWM topologies is analyzed based on the percentages of THD. The THD variation is observed by varying modulation index. From the frequency spectrum it is seen that a large number of frequency components are eliminated So, the THD is reduced in the proposed modified carrier scheme.



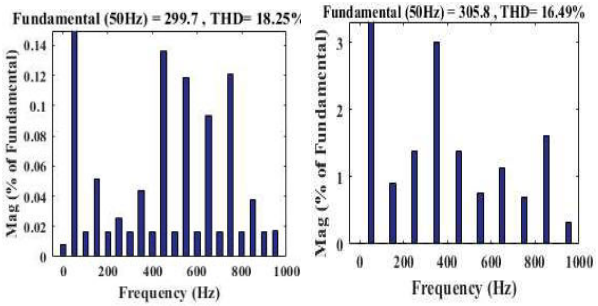
(a) (b)

Fig. 7. Output response of cascaded seven level inverter using (a) conventional carrier APOD (b) modified carrier



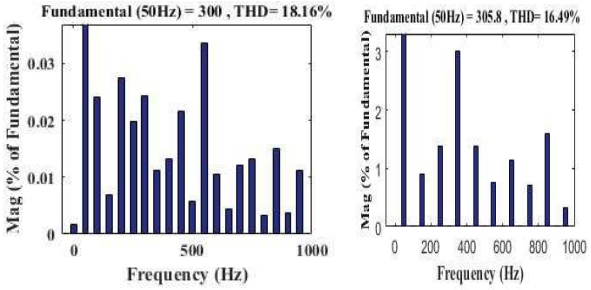
(a) (b)

Fig. 8. Output response of reduced switch seven level inverter using (a) conventional carrier APOD (b) modified carrier APOD.



(a) (b)

Fig. 9. THD spectrum of Output voltage of cascaded seven level inverter using (a) conventional carrier APOD (b) modified carrier APOD.



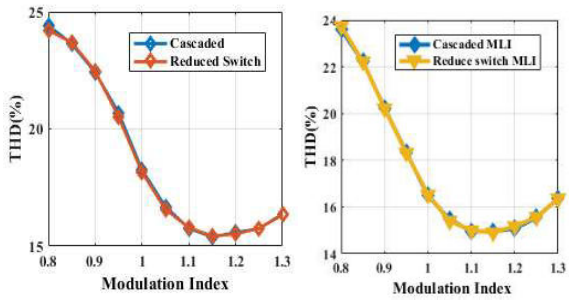
(a) (b)

Fig. 10. THD spectrum of Output voltage of reduced switch seven level inverter using (a) conventional carrier APOD (b) modified carrier APOD.

A. *Conventional carrier based APODPWM*

The performance of conventional APODPWM is evaluated with varying modulation index. The modulation index is varied from range 0.8 to 1.3. While varying modulation index, frequency is kept fixed at

1.5-kHz. Figure-11(a) shows the calculated THD of conventional APODPWM for the variation of modulation index. From the Fig. 11(a), it is shown that at low modulation index percentage of THD is higher. With the increasing modulation index, percentage of THD decreases. After a certain modulation index, THD also increases. It can be seen from Fig. 11(a) that the lowest THD is observed at modulation index 1.15.



(a) (b)

Fig. 11. Calculated THD for (a) conventional carrier APOD (b) modified carrier APOD.

B. *Modified carrier based APODPWM*

The THD variation of modified carrier based APODPWM for modulation index variation is indicated in Fig. 11 (b). Here the lowest THD 14.95 % for cascaded seven level inverter and 14.92% for reduced switch seven level inverter is obtained for modulation index 1.15 when the carrier frequency is fixed at 1.5-kHz. From fig. 11, it is illustrated that the performance of cascaded and reduced switch topologies is almost same for any modulation index.

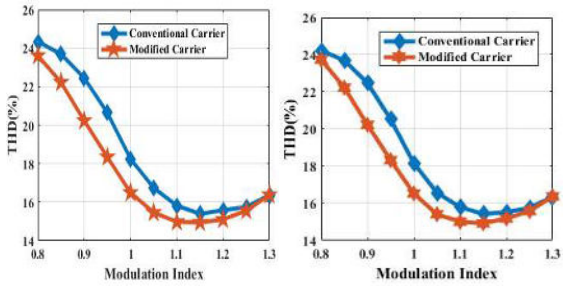
VII. Comparative Analysis

Here, the comparison between conventional carrier and modified carrier based APODPWM topology has been done with the help of simulation results. This comparison has carrier out based on total harmonic distortion (THD), fundamental output voltage and inverter loss.

A. *Total harmonic distortion comparison*

Total harmonic distortion has an adverse effect on equipment and conductor. Higher THD offers increased heating loss, arising false triggering, reduced life time of devices. In addition, it also increases the cost and size of the filtering devices. So it is important to reduce the THD of inverter. The comparative result based percentages of THD has been shown in Fig. 12. The following figure will provide better understanding about the justification of our proposed model.

From the Fig. 12, it is observed that the THD is lower for modified carrier based APODPWM than conventional carrier based APODPWM technique. For fixed carrier frequency 1.5-kHz, the lowest level of THD is observed at modulation index 1.15 for both cascaded and reduced switch seven level inverter. For this modulation index, the THD of our proposed model is lower than conventional carrier based APODPWM.



(a) (b)

Fig. 12. THD comparison for (a) cascaded seven level inverter (b) reduced switch seven level inverter.

B. *Fundamental output voltage comparison*

In this section, the comparison between conventional carrier and modified carrier based level shifted SPWM topologies has been done in terms of fundamental output voltages. The fundamental voltage comparison between two techniques has been shown in TABLE III.

From this table, it is seen that fundamental output voltage increases with increasing of modulation index. For fixed carrier frequency 1.5-kHz and modulation index 0.95, the highest improvement of the fundamental output voltage is obtained for our proposed topology which is around 2.57[%] in compare to conventional topologies. So our proposed topology is better than conventional topology in terms of fundamental output voltage.

C. *Switching loss comparison*

After calculating the switching losses for conventional and modified carrier based APODPWM topology, the simulation results are presented in Fig. 13.

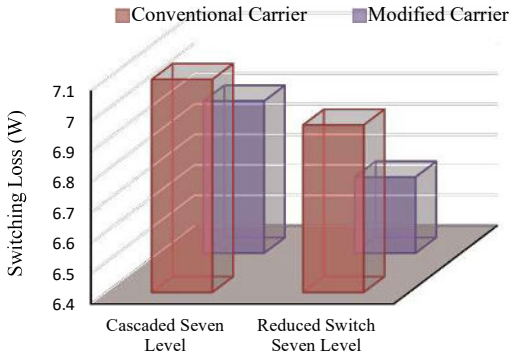


Fig. 13. Switching loss comparison for (a) cascaded seven level inverter (b) reduced switch seven level inverter.

From the above figure, it is undoubtedly shown that the modified carrier based APODPWM offers minimum switching loss in compared to conventional topology. Hence, our proposed topology is also better in terms of switching loss.

TABLE III
FUNDAMENTAL OUTPUT VOLTAGE OF CASCADED AND REDUCED SWITCH SEVEN LEVEL INVERTER USING CONVENTIONAL AND MODIFIED CARRIER BASED APODPWM

Modulation Index	Cascaded Seven Level APOD(RMS)			Reduced Switch APOD(RMS)		
	Conventional	Modified	Improvement (%)	Conventional	Modified	Improvement (%)
0.80	174.7	171.9	-1.6	174.6	174.7	0.6
0.85	185.3	190	2.47	185.3	190	2.54
0.90	195.5	201.6	3.12	195.7	201.6	3.01
0.95	205.8	211.1	2.57	205.7	211.2	2.7
1	215.4	219.2	1.76	215.6	219.2	1.67
1.05	223.1	225.5	1.06	223	225.6	1.17
1.10	228.6	230.6	0.87	228.6	230.7	0.92
1.15	233.2	235	0.77	233.2	235.1	0.81
1.20	237.2	239	0.76	237.2	239	0.76
1.25	240.4	241.6	0.5	240.5	241.6	0.46
1.30	243.5	245.2	0.7	243.5	245.2	0.70

VIII. CONCLUSIONS

In this paper, a modified carrier APODPWM control topology for cascaded and reduced switch seven-level inverter is presented with the help of MATLAB Simulation. According to analysis and comparative study, we can conclude that THD is reduced by 9.64[%] and switching loss is reduced by 4.20[%] in compared to the conventional carrier scheme. Besides, this proposed scheme offers increased fundamental output voltage. The highest improvement in fundamental output voltage is around 2.57[%] in compare to conventional technique when carrier frequency and modulation index are 1.5-kHz and 0.95 respectively. Finally, we can say that the performance of cascaded and reduced switch seven-level inverter can be improved by using modified carrier based APODPWM topology.

REFERENCES

[1] S. Hossain, M.M.Rahman, " A Modified Three and Five Level Cascaded NPC Inverter Topology for Grid Connected PV System" 2019 5th International Conference on Advances in Electrical Engineering (ICAEE), Dhaka, Bangladesh, 2019.

[2] Muhammad H. Rashid, Power Electronics-Circuits, Devices, and Applications, 3rd Edition, PHI Learning Private Limited, 2009

[3] Arif, M. & Md, Shahrin & Iqbal, Atif & Williamson, Sheldon & Salam, Zainal "Nine-level asymmetrical single phase multilevel inverter topology with low switching frequency and reduce device counts" 2017 IEEE International Conference on Industrial Technology (ICIT).

[4] M. T. Islam, M. S. Islam and A. K. Bairagi, "A New Single Phase 21 Level Inverter Topology with Reduced Number of Switches and Sources for Renewable Energy Applications," 2018 4th International Conference on Electrical Engineering and Information & Communication Technology (iCEEiCT), Dhaka, Bangladesh, 2018, pp. 561-565.

[5] M. T. Islam, M. R. Islam, M. S. B. Islam and M. S. Rahman, "Improvement in Performance of Asymmetric Multilevel Inverter Used for Grid Integrated Solar Photovoltaic Systems," 2019 5th International Conference on Advances in Electrical Engineering (ICAEE), Dhaka, Bangladesh, 2019, pp. 91-96.

[6] M. R. Islam, Y. Guo and J. G. Zhu, "Transformer-less local grid based 11 kV SCHB multilevel converter for renewable energy systems," 2011 International Conference on Electrical Machines and Systems, Beijing, 2011, pp. 1-6.

[7] Ashib Rahman, Md Rabiul Islam "Performance evaluation of carrier-based modulation strategies for modular cascaded H-bridge multilevel converters" International Conference on Electrical, Computer and Communication Engineering (ECCE). February 16-18, 2017, Cox's Bazar, Bangladesh.

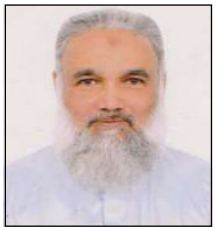
[8] M. Rasheed, R. Omar and M. Sulaiman, "Comparative performance of multilevel inverter for harmonic reduction based on Newton Raphson," 4th IET Clean Energy and Technology Conference (CEAT 2016), Kuala Lumpur, 2016, pp. 1-7.

[9] Nayna Bhargava, Sanjeev Gupta, S. P. Phulambrikar "Analysis of Asymmetrical Cascaded 7 level and 9 level Multilevel inverter design for Asynchronous Motor," International Journal of Engineering Research & Technology Vol. 3 Issue 8, August-2014.

[10] T. Sengolrajan, B.Shanthi, S.P. Natarajan, "Comparative Study of Multicarrier PWM Techniques for Seven Level Cascaded Z-Source Inverter International Journal of Computer applications, Engineering Systems Vol. 65, No. 6, pp. 45-53, 2010.

[11] Chinnathambi Govindaraju and Kaliaperumal Baskaran, "Power Loss Minimizing Control of Cascaded Multilevel Inverter with Efficient Hybrid Carrier Based Space Vector Modulation," International Journal of Electrical and Computer Engineering Systems, Vol. 1, No. 1, pp. 45-53, 2010.

Md. Tariqul Islam was born in Naogaon. He has completed his graduation in Electrical and Electronic Engineering (EEE) from Rajshahi University of Engineering and Technology (RUET), Bangladesh in 2018. Currently, he has been working as a Lecturer of EEE department in Green University of Bangladesh (GUB), Dhaka. He has contributed to a good number of published technical articles including international journals, international conference proceedings as well as. His interested research field includes power converter, grid integration of renewable energy sources, power electronics, and solid state transformer.



Md. Fayzur Rahman was born in 1960 in Thakurgaon, Bangladesh. He received the B. Sc. Engineering degree in Electrical & Electronic Engineering from Rajshahi Engineering College, Bangladesh in 1984 and M. Tech degree in Industrial Electronics from S. J. College of Engineering, Mysore, India in 1992. He received Ph. D. degree in energy and environment electromagnetic from Yeungnam University, South Korea, in 2000. He was a Professor in Electrical & Electronic Engineering in Rajshahi University of Engineering & Technology (RUET) and served as HOD of the same department. He also served as departmental head for two years in EEE department and 2 years in ETE department of Daffodil International University. After that he joined in the EEE department of Green University of Bangladesh on January 2016 and served as Chairperson of the EEE department for 4 years. At present, he is working as a professor in the same department. His current research interests are Energy and Environment Electromagnetic, Power Electronics & Machine Control and High Voltage Discharge Applications. He is a fellow of the Institution of Engineer's (IEB), Bangladesh and Life member of Bangladesh Electronic Society.

Dr. A. A. Md. Monzur-Ul-Akhir was born in Dhaka. He is currently acting as an Assistant Professor in Electrical and Electronic Engineering Department, Green University of Bangladesh. He is also acting as an Associate Editor of the Green University of Bangladesh Journal of Science and Engineering (GUBJSE). He is an ex-Notredamian. He completed his Bachelors and Masters in EEE from the University of Dhaka. He also completed his MBA in Finance from the Institute of Business Administration (IBA) from the University of Dhaka in 2012. He got the prestigious merit scholarship from the Japanese Government-Monbukagakusho (Monbusho/MEXT) in 2014 to pursue his PhD in Nano and Functional Material Sciences from the University of Toyama. After his Ph.D. degree in 2018 he was then awarded with the "Marubun Research Promotion Foundation Grant 2017" to complete his Postdoctoral research from 2018-2019 at the University of Toyama. His research interest includes Group III-V Compound Semiconductors, Thin-film growth, Spintronics, Solar cell, Solar Materials, Nanotechnology, Cryptography, Robotics, Electronic devices, Business studies, etc. He attended the international conference ICIEV 2019, Washington, Spokane, USA, and his submitted paper won the best paper award. He has several journal and conference publications.

Zisun Ahmed received his bachelor's in electrical and electronic engineering (EEE) from Ahsanullah University of Science and Technology and his master's in biomedical physics and technology (BMPT) from the University of Dhaka (DU). After working as a research engineer at the department of BMPT (DU), he joined biomedical micro device lab at Hong Kong University of Science and Technology (with Prof. Levent Yobas) to conduct research on ion concentration polarization in 1-D nanocapillaries and received his M.Phil in Bioengineering in 2019. He has been working as a Lecturer of EEE department in Green University of Bangladesh since January 2020.