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SELF-ASSEMBLE MONOLAYER DEPENDENT FIELD EFFECT TRANSISTOR'S PERFORMANCE BASED ON TETRACENE SINGLE-CRYSTAL

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Abstract

Organic field effect transistors with an active layer based on the tetracene single-crystal were fabricated. It was found that organosilane self-assemble monolayer (SAM) modified device with tetracene single-crystals gave higher mobility and on/off ratio rather than untreated device. SAM modified tetracene single-crystal transistors with parylene gate insulator showed the highest mobility of 0.66 $cm^2 V^{-1} s^{-1}$ and high on/off ratio of ~ 10^4. This finding demonstrates that SAM treatment decrease the charge leakage between source and drain which help to decrease the off current with greater extent and increase the on current slightly of the tetracene single-crystal field-effect transistors.

Introduction

Organic semiconductors have been recently attracted much attention for their applications in organic field-effect transistors (OFETs) and significant progress has been made in OFET performance.[1] Organic semiconductors such as oligoacenes, oligothiophenes and their derivatives have been studied as fundamental building blocks for OFET.[2] Most of the research has been performed on thin film transistors (TFTs),[3] because majority of unsubstituted conjugated organic oligomers exhibit good crystalline film forming properties. These molecules typically crystallize in herringbone packing motif, in which π-orbital repulsion is minimized by the 2D edge-to-face molecular arrangement resulting in better polycrystalline films. The highest charge carrier mobility in polycrystalline films has been achieved with pentacene used as a benchmark semiconductor material with the highest reproducible mobility of ~ 1 $cm^2V^{-1} s^{-1}$. The performance of TFT devices mainly depends on film morphology and it depends on many parameter like molecular structure of semiconductor, nature of substrate, thin film deposition temperature and deposition rate etc. Organic single-crystal transistors have been developed as an ideal tool for the exploration of charge transport in organic semiconductors.[5] Research in single-crystal FETs (SCFETs) has been intensifying due to their advantages in studying the intrinsic carrier transport properties, free from extrinsic effects of grain boundaries, molecular disorder and associated with them charge traps.[6]

In general, silicon dioxide (SiO_2) is used as gate insulator in the OFETs though organic FETs on bare SiO_2 suffer from several problems which depend on the nature of the semiconductor/SiO_2 interface.[7] It is wellknown that SiO_2 surface contains defect sites which can trap charge in the channel.[8] The self-assemble monolayer (SAM) of organosilane compounds is used as buffer layer between the semiconductor active layer and the gate insulating layer in organic FETs to reduce the charge trapping sites, which

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influence the OFET performance.[9,10,11] The device performance of organic FETs is strongly dependent on the nature of SAM molecules. Recently parylene gate insulator is used as interfacial layer in organic single-crystal transistors due to its smooth surface as the charge transport in organic FETs takes place through the first few layers of semiconductor near the semiconductor/gate insulator interface.[12,13] The great advantage of parylene gate insulator is it does not react with organic semiconductors.

In this work, we report the single-crystal FETs characteristics of tetracene using self-assemble monolayer (SAM) treated substrate which exhibits very high mobility of 0.66 $cm^2\ V^{-1}\ s^{-1}$ rather than untreated device (0.38 $cm^2\ V^{-1}\ s^{-1}$) and high on/off ratio of ~ 10^4 than untreated one (up to 10^2).

Experimental

Single-Crystal growth

Plate and ribbon like crystals of tetracene were grown by physical vapour transport method[14] in the presence of a stream (30cc/min) of ultra pure argon at 220^0C. Tetracene was purchased from Aldrich and used without further purification. First and second time grown crystals were resublimed to get more pure crystals as the device performance also depends on the crystal quality.[15] Purchased tetracene actually not 100% pure and it is easily oxidized in atmosphere. When resublime it, we found some residue in sublimation boat at every time though the crystal was look like same and we do not find any change in UV data. Photograph of tetracene crystals is shown in Fig. 1 which is taken by digital camera using normal mode. In this Fig. shape and color of the tetracene crystals are shown clearly. Crystal thickness actually depends on time, argon flow rate and temperature. Tetracene crystals with thickness of 10 – 80 μm were found and crystal thicknesses of 40 – 80 μm were used in our device. Tetracene adopt herringbone molecular packing arrangements with an edge-to-face pattern.[16,17]

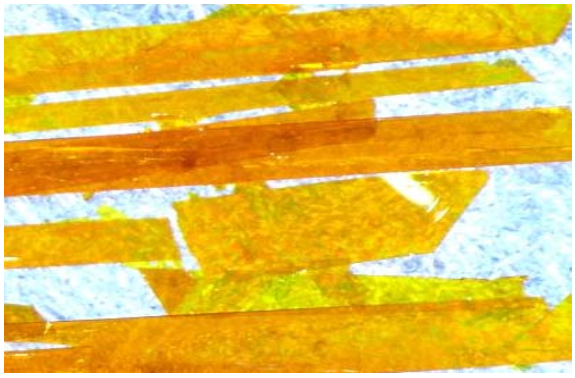

Fig. 1. Digital photograph of tetracene single-crystals.

Device Fabrication

The device substrates were cleaned in piranha solution (H_2SO_4/H_2O = 4:1) then through washed with de-ionized (DI) water and put in an ultrasonic bath for 5 min with DI water and washed again with water. Finally, the washed substrates were dried with stream of nitrogen. The cleaned substrates were placed in 10 mM of n-octadecyltrichlorosilane (ODTS) solution in dry toluene for 3 min to make a self-assemble monolayer (SAM), and after removing the substrates from the solution it was washed with dry toluene dried by the stream of nitrogen. ODTS monolayer is usually used in thin film transistors to improve the device performance.[18] The reported thickness of ODTS self-assembled monolayer is 2.6 nm.[19] The origin of improvement is complicated due to its effect on the thin film morphology.[20] Top-gate/top-contact tetracene single-crystal devices were fabricated (Fig. 2). Colloidal graphite was used as source, drain and gate contacts; parylene used as dielectric gate insulator.[21] Thickness of source, drain and gate contact were not measured. To minimize the trap density, parylene used as gate dielectric insulator for FETs fabrication.[22,23] The graphite was painted on the smooth untreated tetracene single-crystal surface. The channel length (L) and width (W) (Fig. 2) were 1.0 - 0.45 mm and 0.50 - 0.20 mm respectively. Parylene was deposited on the tetracene single-crystal with preformed source and drain contacts in a homemade reactor. Finally colloidal graphite was painted on the top of the parylene over the region between the source and drain as a gate electrode. Parylene film thickness was measured with alpha step. The measured parylene thickness was 1.25 - 2.35 μm.

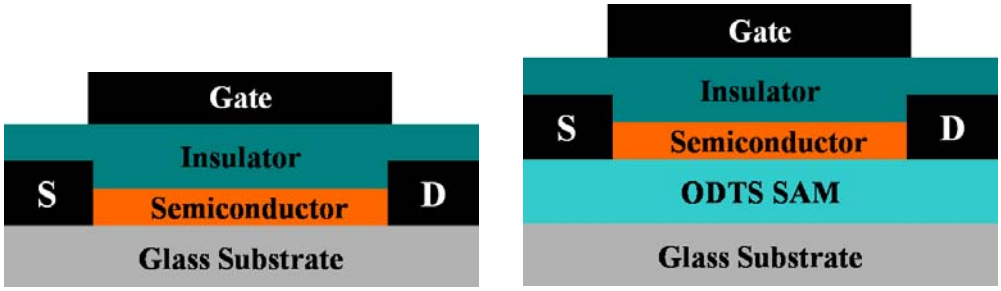

Fig. 2. Schematic diagram of tetracene single-crystal field effect transistors (a) with bare substrate and (b) with ODTS/substrate.

Results and Discussion

The electrical characteristics of the tetracene single-crystal FETS were measured in a dark chamber using a computer controlled Agilent HP4156 semiconductor parameter analyzer at ambient condition. The transistors were operated in the accumulation mode by applying a negative gate voltage. The source electrode was grounded, and the drain electrode was negatively biased between 0 and -80 V. Typical output and transfer

characteristics of tetracene single-crystal FETs are shown in Fig. 3. It shows the p-type electrical characteristics of the tetracene single-crystal FETs. The drain current exhibited a good saturation at different gate voltages at high drain voltages (Fig. 3 (a) and (b)). In Fig. 3(d) the device off current is very low with compare to off current of device without SAM (Fig. 3c). As a result the on/off ratio of device with SAM is higher than device without SAM. The upper graph (Fig. 3(d)) is more bending than lower one due to very low off current. The charge carrier mobilities were calculated in the saturation regime according to the equation

$$I_{ds} = \frac{W}{2L} C_i \mu (V_g - V_{th})^2$$

where μ is the carrier mobility, C_i is the gate capacitance per unit area, W and L are the channel width and length, I_{ds} is the source drain current, V_g is the gate voltage, and V_{th} is the threshold voltage.

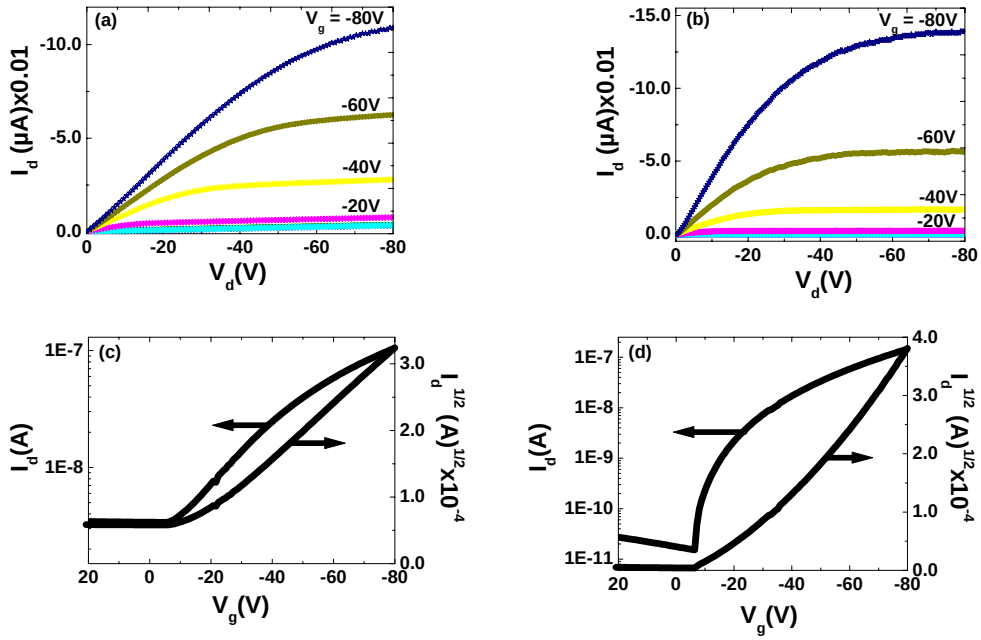

Fig. 3. Electrical characteristics of tetracene single-crystal FETs: (a) and (b) output characteristics, (c) and (d) transfer characteristics with bare and ODTS modified substrate respectively.

The output characteristics show well-developed saturation regime at several gate voltages. Hole mobilities as high as 0.66 $cm^2 V^{-1} s^{-1}$ with an on/off ratio of ~ 10^4 has been measured for ODTS SAM-modified devices in saturation regime at ambient conditions. This high value was achieved due to the SAM modified substrates. The performance of

the transistors was highly reproducible. Morpurgo group also reported the single-crystal FET mobility of tetracene up to 0.4 cm^2 V^{-1} s^{-1} using the same device pattern without SAM.[18] Our results suggest that the charge leakage between source and drain is an important parameter for organic semiconductors which greatly influenced the device performance. We have performed a control experiment with and without ODTS SAM with the same device configuration in the absence of a semiconductor. The measured current for without SAM is in the order of 10^{-8} A, whereas on an ODTS-modified substrate, the current dropped to 10^{-10} A (Fig. 4). This charge leakage reduces the on/off ratio of the device. The leakage may be due to charge conduction on the hydroxyl surface with adsorbed moisture.

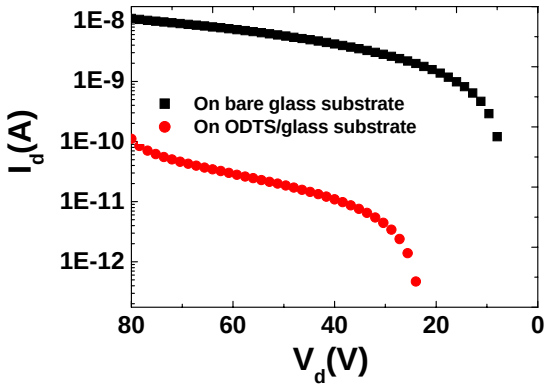

Fig. 4. I_{ds} vs. V_{ds} curves for bare glass and ODTS-modified glass substrate**.**

Conclusion

In conclusion, we have studied the transistor operation of single-crystal FETs based on tetracene that has a edge to face π-conjugated framework using ODTS self-assemble monolayer (SAM) modified substrate. SAM treated tetracene single-crystal FETs exhibited the higher charge carrier mobilities up to 0.66 cm^2 V^{-1} s^{-1} and high on/off ratio up to 10^4 than untreated FETs (up to 0.38 cm^2 V^{-1} s^{-1} and high on/off ratio up to 10^2) in ambient conditions. The performance of these transistors was highly reproducible. These results indicate that the untreated FETs have charge leakage between source and drain which help to increase the high off current and slightly decrease the on current. Further microscopic studies are required to get more information about function of SAM on organic field effect transistors.

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I_d (μA)x 0.01	I_d (μA)x 0.01	V_d(V)	V_d(V)	V_g(V)	V_g(V)	I_d(A)	V_d(A)
I_d (μA)x 0.01	I_d (μA)x 0.01	V_d(V)	V_d(V)	V_g(V)	V_g(V)	I_d(A)	V_d(A)

$I_d^{1/2}$ $(A)^{1/2}$ x 10^{-4}

$I_d^{1/2}$ $(A)^{1/2}$ x 10^{-4}