

## Tetracene Based OTFT with $\text{Nd}_2\text{O}_3$ -dielectric Layer

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### Abstract

Tetracene thin film transistors with rare earth oxide ( $\text{Nd}_2\text{O}_3$ ) as gate dielectric is reported in this work. Rare earth oxide with high dielectric constant and low leakage current improve the performance of the organic thin film transistors (OTFTs). The fabricated tetracene OTFTs have shown good output characteristics with mobility  $0.93 \times 10^{-4} \text{ cm}^2/\text{V}\cdot\text{s}$ , ON-OFF ratio  $3.3 \times 10^2$ , sub-threshold swing  $0.06 \text{ V/decade}$  and hole concentration  $8.74 \times 10^{17} \text{ cm}^{-3}$ .

*Keywords:* Organic thin film transistors; Tetracene; Rare earth oxide; Trap density.

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### 1. Introduction

Organic thin film transistors (OTFT) are currently the subject of substantial international research, with much potential in commercial applications such as flexible display panel [1, 2], chemical sensors [3, 4], electronic paper [5]. Compared to traditional silicon devices, they have low production costs; much of the processing can be performed at or near room temperature; and the techniques involved tend to be simpler than for silicon. Compared with a conventional non-organic transistor, the OTFT can be constructed at a lower temperature. In addition, the organic thin film transistor involves simpler manufacturing processes [4] that do not require certain high precision technique and equipment. In this regard, the OTFT are of great potential and interest for further development. Although the organic thin film transistor has the advantages as described above, there are still some bottlenecks choking such as low carrier mobility and high driving voltage.

The organic materials that have been used as active semiconductor materials in OTFTs include both oligomers [6, 7] and polymers [8]. An organic semiconductor is an organic

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compound that possesses similar properties to inorganic semiconductors with hole and electron conduction layer and a band gap [9]. Organic semiconductors differ from other organic materials in that the molecules have  $\pi$  conjugate bonds which allow electrons to move via  $\pi$ -electron cloud overlaps.

A schematic diagram of the OTFT configuration is shown in Fig. 1. OTFT of short chain (oligomers) organic semiconductors can be prepared by vacuum evaporation method while OTFT long chain (polymers) molecules can be prepared by spin coating method.

Rare earth oxides such as  $\text{La}_2\text{O}_3$ ,  $\text{Pr}_6\text{O}_{11}$ ,  $\text{Nd}_2\text{O}_3$  were reported [10] for next generation high-k gate insulator, and they showed excellent electrical properties such as high dielectric constant and small equivalent oxide thickness (EOT) with low leakage current density. We have already successfully fabricated tetracene OTFTs with  $\text{La}_2\text{O}_3$  gate insulator [11] and pentacene OTFTs with  $\text{Pr}_6\text{O}_{11}$  insulator [12]. In this work we have used  $\text{Nd}_2\text{O}_3$  as gate insulator (Figs. 2).

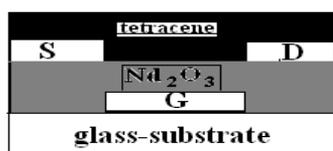


Fig. 1. A schematic illustration of a tetracene-OTFT configuration.



Fig. 2. Photograph of the fabricated tetracene OTFTs.

## 2. Experimental Details

In this present work, the TFTs were prepared by multiple pump down (MPD) method. Using this method, each film of the TFT will be laid down on an insulating substrate, which is glass in our case, using proper masks. After each deposition, the vacuum is broken and the entire TFT is grown in step by step by using the masks of desired shape.

We first deposited metal (Al) gate electrode of thickness  $1120 \text{ \AA}$  on a glass substrate, above which a dielectric layer of  $\text{Nd}_2\text{O}_3$  of thickness  $1160 \text{ \AA}$  is deposited. In the next step source drain electrodes of aluminum (of thickness  $1200 \text{ \AA}$ ) having a channel length  $50 \mu\text{m}$  (using wire grill) were deposited, finally a tetracene semiconductor layer of thickness  $440 \text{ \AA}$  was deposited at vacuum better than  $8 \times 10^{-6}$  torr.

## 3. Results and Discussions

In Fig. 3 we have plotted variation of drain current ( $I_D$ ) with drain voltage ( $V_D$ ) at various gate voltage. In the figure we also compare experimental values with the theoretical values (calculated with Eq. 1) and it is seen that they almost agree with one another which established the reliability of the fabricated device.

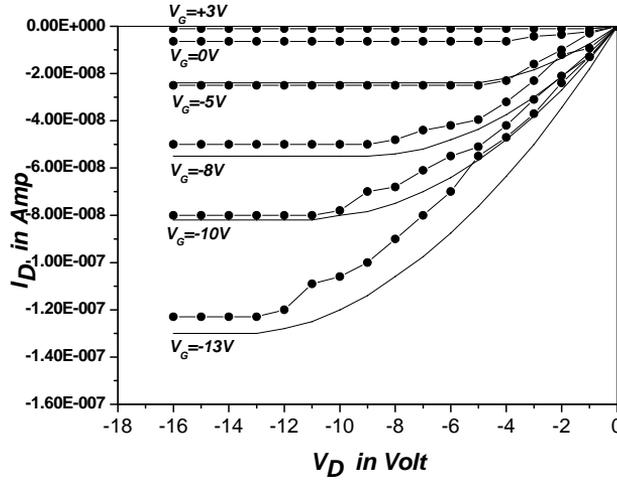


Fig. 3. Variation  $I_D$  vs  $V_D$  (dotted lines indicate experimental variations while smooth lines indicate theoretical variations).

The increase in current with the negative gate voltage indicates field-effect-induced hole conduction, which is the expected behaviour for tetracene. The theoretical equation for drain current ( $I_D$ ) is [13]:

$$I_D = \frac{w}{L} \mu c_i \left( V_G - V_T - \frac{V_D}{2} \right) V_D \quad (1)$$

where  $w$  is the channel width,  $L$  is channel length,  $C_i$  is the capacitance per unit area of the gate insulator,  $V_T$  is the threshold voltage and  $\mu$  is the mobility.

In Fig. 4 we have plotted the variation of saturated drain current ( $I_{Dsat}$ )<sup>1/2</sup> vs. gate voltage  $V_G$  for the high negative gate voltage the variation is almost linear while for the low negative voltage the plot shows unusual results. The slope of the linear region of the plot ( $I_{Dsat}$ )<sup>1/2</sup> vs.  $V_G$  gives the mobility  $\mu$  and the extrapolation of the linear region of the plot to the  $V_G$  axis gives the threshold voltage  $V_T$  [13]. The observed threshold voltage is 1.2V. The positive threshold voltage for p-channel devices may indicate the presence of unwanted p-dopant in the organic layer, thus a positive  $V_G$  is needed to switch off the device [14]. The calculated mobility value with Eq.2 is  $0.93 \times 10^{-4} \text{ cm}^2/\text{V.s}$ .

$$I_{Dsat} = \frac{w}{2L} \mu c_i (V_G - V_T)^2 \quad (2)$$

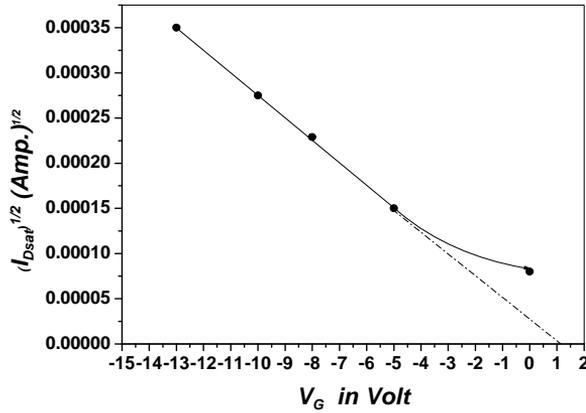


Fig. 4. Plot of  $(I_{Dsat})^{1/2}$  vs  $V_G$ .

The sub-threshold swing is calculated from the slope of the graph shown in Fig. 5 using the relation [15]:

$$s = \left( \frac{d(\log I_D)}{dV_G} \right)^{-1} \tag{3}$$

The calculated value of sub-threshold swing is 0.06 V/decade. Normalizing [16] this value to the capacitance of the dielectric gives 30 VnF/decade.cm<sup>2</sup>. These values are comparable to what is found for the best pentacene TFTs (15-80 VnF/decade.cm<sup>2</sup>) [17, 18].

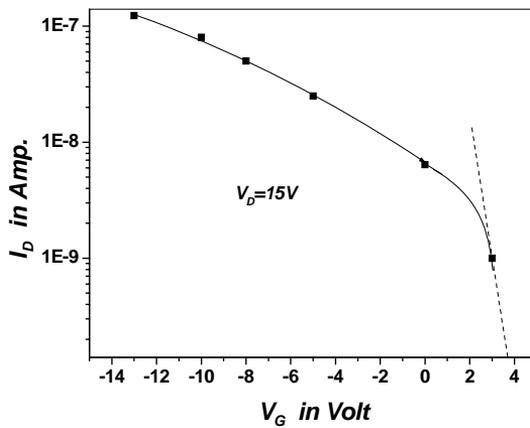


Fig. 5.  $\text{Log}_{10}(I_D)$  vs.  $V_G$  characteristics for the tetracene TFT at  $V_D=15V$ .

The maximum number of interface traps (or trap density) present is estimated using the following relation assuming that the densities of the deep bulk states and interface states are independent of energy [19]:

$$N_{ss}^{\max} = \left\{ \frac{s(\log e)}{KT/q} - 1 \right\} \frac{C_i}{q} \quad (4)$$

The estimated value is  $0.074 \times 10^{11} \text{eV}^{-1} \text{cm}^{-2}$ . The channel conductivity  $\sigma$  is estimated from the plot of  $I_D$  vs.  $V_D$  graph at zero gate voltage. The ON-OFF ratio is estimated from the following relation [13]:

$$\frac{I_{ON}}{I_{OFF}} = \frac{c_i \mu (V_G - V_T)^2}{\sigma d V_D} \quad (5)$$

The estimated value of on-off ratio is  $3.3 \times 10^2$ .

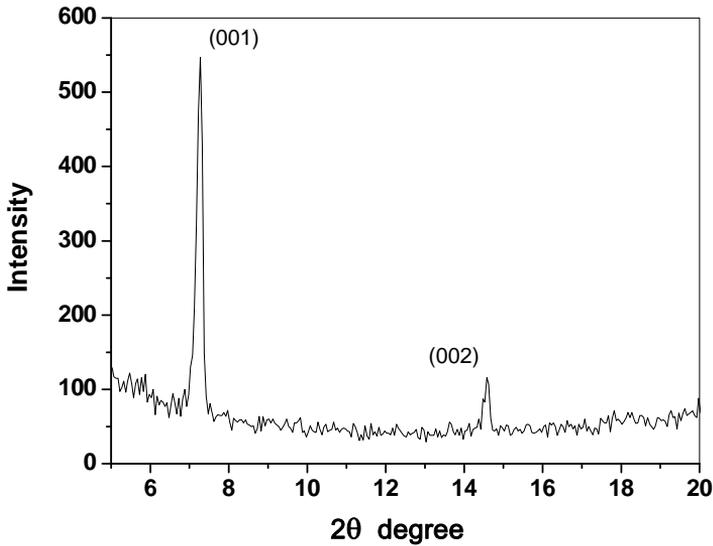


Fig. 6. XRD pattern of the tetracene thin film deposited on glass substrate.

The XRD of the tetracene film is shown in Fig. 6. The Bragg's peaks at (001) and at (002) indicate that the tetracene molecules are packed parallel to each other in a nearly vertical direction where  $c$ -axis of the tetracene molecules are aligned perpendicular to the substrate. The report established that the tetracene films are polycrystalline in nature and is composed of linear chain of identical crystallites.

The various values of the parameter used and evaluated are tabulated in Table 1.

Table 1. The various parameters used and evaluated.

Channel width ( $w$ )	0.14 cm
Channel length ( $L$ )	0.005 cm
Capacitance per unit area ( $c_i$ )	0.005 F/m <sup>2</sup>
Channel thickness ( $d$ )	440 Å
Threshold voltage ( $V_T$ )	1.2 V
Channel Mobility ( $\mu$ )	$0.93 \times 10^{-4}$ m <sup>2</sup> /V.s
Channel Conductivity ( $\sigma$ )	$1.3 \times 10^{-5}$ Ω <sup>-1</sup> cm <sup>-1</sup>
Sub threshold swing ( $s$ )	0.06 V/decade
$I_{ON} / I_{OFF}$	$3.3 \times 10^2$
Hole concentration ( $N_p$ )	$8.74 \times 10^{17}$ cm <sup>-3</sup>
Maximum numbers of interface traps present ( $N_{ss}^{max}$ )	$0.74 \times 10^{11}$ eV <sup>-1</sup> cm <sup>-2</sup>

#### 4. Conclusions

The fabricated OTFTs have well defined  $I$ - $V$  characteristics. ON-OFF ratio of the OTFTs better than  $3.3 \times 10^2$ . The normalizing value of sub-threshold swing to the capacitance of the dielectric is 30VnF/decade.cm<sup>2</sup>, which is comparable to what is found for the best pentacene TFTs (15-80VnF/decade.cm<sup>2</sup>) [17, 18]. These results can be considered as satisfying for tetracene OTFT with Al-electrodes. The values can be further improved using Au-source drain electrode which offers less contact resistance than Al-electrodes.

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#### References

1. M. Mizukami, N. Hirohata, T. Iseki, K. Ohtawara, T. Tada, S. Yagyu, T. Abe, T. Suzuki, Y. Fujisaki, Y. Inoue, S. Tokito, and T. Kurita, IEEE Electron Device Lett. **27** (4), 249 (2006). [doi:10.1109/LED.2006.870413](https://doi.org/10.1109/LED.2006.870413)
2. S. Ono and Y. Kobayahi, Jpn. J. Appl. Phys. **43** (12), 7947 (2004). [doi:10.1143/JJAP.43.7947](https://doi.org/10.1143/JJAP.43.7947)
3. F. Liao, C. Chen, and V. Subramanian, Sensors and Actuators B: Chemical **107**, 849 (2005). [doi:10.1016/j.snb.2004.12.026](https://doi.org/10.1016/j.snb.2004.12.026)
4. M. Halik, H. Klauk, U. Zschieschang, G. Schmid, C. Dehm, M. Schütz, S. Maisch, F. Effenberger, M. Brunnbauer, and F. Stellacci, Nature **431**, 963 (2004). [doi:10.1038/nature02987](https://doi.org/10.1038/nature02987)
5. S. H. Han, S. M. Cho, J. H. Kim, J. W. Choi, and J. Jang, Appl. Phys. Lett. **89**, 093504 (2006). [doi:10.1063/1.2338526](https://doi.org/10.1063/1.2338526)
6. A. L. Briseno, S. C. B. Mannsfeld, M. M. Ling, S. Liu, R. J. Tseng, C. Reese, M. E. Roberts, Y. Yang, and F. Sacuto, Phys. Rev. B **70**, 081309(R) (2004).

8. H. Yan, Z. Chen, Y. Zheng, C. Newman, J. R. Quinn, F. Dötz, M. Kastler, and A. Facchetti, *Nature* **457**, 679 (2009). [doi:10.1038/nature07727](https://doi.org/10.1038/nature07727)
9. G. Horowitz, *Advanced Materials* **2**, 287 (1990). [doi:10.1002/adma.19900020604](https://doi.org/10.1002/adma.19900020604)
10. H. J. Osten, J. P. Liu, P. Gaworzewski, E. Bugiel, and P. Zaumseil, *IEDM Tech. Dig.* 653 (2000). [doi:10.1103/PhysRevB.70.081309](https://doi.org/10.1103/PhysRevB.70.081309)
11. R. Sarma and D. Saikia, *Indian J. Pure & Appl. Phys.* **47**, 876 (2009).
12. R. Sarma, D. Saikia, and B. Barua, Organic Thin Film Transistor with Pr<sub>6</sub>O<sub>11</sub>-dielectric layer (poster presentation- 42), *In: Indo-Russian Workshop on Nanotechnology and Laser Induced Plasma Proceedings (IRNANO-2009)*.
13. B. C. Shekar, J. Lee, and Shi.-W. Rhee, *Korean J. Chem. Eng.* **21**, 267 (2004). [doi:10.1007/BF02705409](https://doi.org/10.1007/BF02705409)
14. N. Koch, *Chem Phys Chem*, **8**, 1438 (2007). [doi:10.1002/cphc.200700177](https://doi.org/10.1002/cphc.200700177)
15. J. H. Seo, J.-H. Kwon, S.-H Shin, K.-S. Suh, and B.-K. Ju, *Semicond. Sci. Technol.* **22**, 1039 (2007). [doi:10.1088/0268-1242/22/9/011](https://doi.org/10.1088/0268-1242/22/9/011)
16. R. W. I. de Boer, T. M. Kalpwijk, and A. F. Morpurgo, *Appl. Phys. Lett.* **83**, 4345 (2003). [doi:10.1063/1.1629144](https://doi.org/10.1063/1.1629144)
17. D. J. Gundlach, J. A. Nichols, L. Zhou, and T. N. Jackson, *Appl. Phys. Lett.* **80**, 2925 (2002). [doi:10.1063/1.1471378](https://doi.org/10.1063/1.1471378)
18. Y. Y. Lin, D. J. Gundlach, S. F. Nelson, and T. N. Jackson, *IEEE Trans. Electron Devices* **44**, 1325 (1997). [doi:10.1109/16.605476](https://doi.org/10.1109/16.605476)
19. A. Rollend, J. Richard, J. P. Kleider, and D. Mencaraglia, *J. Electrochem. Soc.* **140**, 3679 (1993). [doi:10.1149/1.2221149](https://doi.org/10.1149/1.2221149)