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Study on the On/Off Ratio of the Cylindrical Surrounding Gate CNT Transistor Using Nonequilibrium Green's Function Approach

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Abstract

The effects of the nanotube diameter, channel length, gate dielectric constant and gate dielectric thickness on the on-off current ratio performance of cylindrical surrounding gate carbon nanotube transistors are studied using a π-orbital tight binding simulation model. The focus is both on Schottky barrier and the doped source-drain contact devices. The on current significantly improves with high-κ gate dielectric, whereas off current decreases. The device on-off current ratio improves, from 6.33×10^5 to 1.5×10^6 for doped contact and from 0.61×10^4 to 1.22×10^4 for SB device with thinner gate oxide. Minimum leakage current increases with larger diameter tube but on-current has no significant improvement. I-V characteristics are independent of channel length when it is larger than 15 nm. Significant increase in off-current occurs due to scaling the channel length down to 10 nm but on-off ratio still exceeds 10^3. In all cases, on-off ratio is higher and the effect of scaling is more prominent for doped contact devices than SB contact devices.

Keywords: Carbon nanotube; Transistor; NEGF; On-off Ratio.

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1. Introduction

A higher integration density has come out as a result of aggressive scaling of CMOS devices over different technology generations. However, scaling of the devices beyond 10 nm is affected by "short channel effects" such as exponential increase in leakage current and large parameter variations [1]. CMOS will reach its performance limits by 2020, as predicted by the International Technology Roadmap for Semiconductors (ITRS) [2]. Therefore, search for alternatives to MOSFETs in sub-10 nm regime have started through

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research. Single electron transistors [3], silicon nanowire transistors [4, 5], and carbon nanotube field-effect transistors (CNTFETs) [6] have been proposed as candidates for future electron devices. There has been remarkable progress in performance and physical understanding of CNTFET [7] since their first demonstration in 1998 [8]. For low-bias conditions at low temperatures ballistic transport in CNTs has been demonstrated experimentally [9]. High-performance CNT transistors operating close to the ballistic limit has also been reported [10, 11]. Exceptional device characteristics can be expected as the experimentally obtained carrier mobilities are in the order of 10^4 cm^2/V.s [12]. Significant progress has been made in fabrication process of CNT such as separating the semiconducting and metallic tubes [13] and controllable deposition techniques [14] and CNT thin film deposition [15]. Integration of high-κ gate dielectric insulator [16, 17] and use of excellent source and drain metal contacts [10] has been demonstrated with improvement in performance. Transistors with exceeding performance to the state of the art, Si MOSFET are achieved. The transistor delivers a current of ~ 20 μAat $|V_G - V_T|$ ~ 1V and has a near-ballistic source-drain conductance of ~ $0.5 \times 4e^2/h$.

Two structures have been recommended in literature for CNTFETs. In one structure CNT channel is directly connected with two metal electrodes at both ends. Schottky barriers are formed at the metal electrode junctions. This structure is known as SB-CNTFET. This device is operated by modulation of the tunneling barrier at the source contact. The other structure also uses a single-wall CNT as CNT channel. But in this structure a portion of the channel adjacent to the metal electrodes are heavily doped. This device is known as MOSFER-like CNTFET and the transport mechanism is based on modulation of the barrier height of the conduction band between source and channel regions. Conventional CNTFET with lower leakage current along with high on state current at ballistic regime compared to Schottky barrier CNTFETs (SB-CNTFETs) has been reported recently [6].

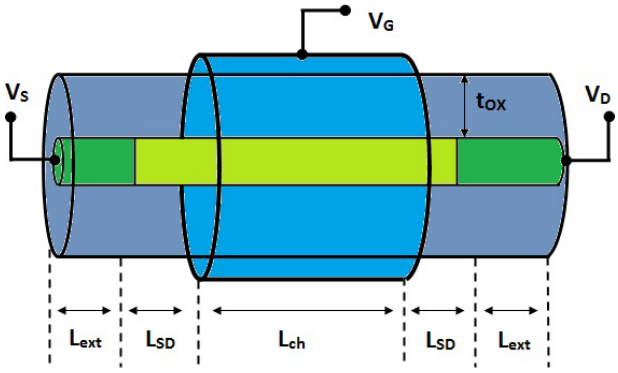


Fig.1. The structure of the device with surrounding gate.

On/off ratio is an important performance parameter of FET. To minimize static power dissipation a low off-current is required. On the other hand, high on-current reduces the gate switching delay. Therefore a high on/off current ratio improves device performance.

The objective of this research work is to investigate the effect of gate dielectric constant κ, dielectric thickness t_{OX}, diameter d, channel length L_{ch} on the on/off ratio of cylindrical gate CNTFET using two simulation tools named CNTFETLab and Cylindrical CNTMOSFET simulator [18, 19]. Here, we focus on both doped contact device and Schottky barrier contact.

2. Experimental

2.1. *CNTFET device structure*

The geometry of the device has source and drain regions (L_{SD}) and a cylindrical wrap-around metallic gate electrode over the intrinsic channel region (L_{ch}) as shown in Fig. 1. The gate oxide with thickness t_{OX} covers the full length of the tube. L_{ext} are artificial heavily doped extension regions. These extension regions do not influence the transport in the working part of the transistor but are useful for better numerical convergence purposes. The transistor channel is a (13, 0) intrinsic CNT, which results in a band gap of ~ 0.82eV and a diameter of ~ 1.01 nm. The nanotube length is ~ 20 nm, consisting of ~ 3.9×10^3 carbon atoms. Other device parameters used for the simulation are as follows: source/drain length, LSD = 30 nm, gate oxide thickness t_{OX} = 2 nm (HfO_2 with k=16), the source/drain doping NSD = 1.5/nm. These are the nominal parameters as suggested by Lundstrom *et al.* [20], used throughout our simulation unless specified otherwise. A self-consistent Poisson-NEGF simulation in the mode space using the recursive algorithm for computing the Green's function is performed as illustrated in next section.

2.2. *Simulation approach*

Simulation is done by numerically solving the Schrödinger and Poisson equations self-consistently utilizing nonequilibrium Greens function formalism (NEGF) [21]. *k*-Space approach is used instead of real space to reduce the computational cost [20]. The device Hamiltonian used in this work is based on the atomistic nearest neighbor p_Z-orbital tight-binding approximation. NEGF modeling of CNTFETs considering ballistic transport is described elsewhere [20, 22].

The retarded Greens function for the device in matrix form is given by,

$$G(E) = [(E + i\eta^+)I - H_{pz} - \Sigma(E)]^{-1} \quad (1)$$

Where, η^+ is an infinitesimal positive value, and I is the identity matrix. The self-energy contains contributions from all mechanisms of relaxations, which are the source and drain electrodes, and from scattering,

$$\Sigma(E) = \Sigma S(E) + \Sigma D(E) + \Sigma_{Scat}(E) \quad (2)$$

The description of the Hamiltonian matrix H_{pz} is given in [22, 20]. Under ballistic condition the current from drain to source is given by,

$$I = \frac{4e}{h}\int_{-\infty}^{+\infty}\frac{dE}{2\pi}T(E)[f(E-E_S^F)-f(E-E_D^F)] \quad (3)$$

With the transmission coefficient *T(E)* given by,

$$T(E) = Trace[\Gamma S(E)G(E)\Gamma D(E)G\dagger(E)] \quad (4)$$

Equation (4) is the famous Landauer equation that is widely used in mesoscopic transport [20]. The electrostatic potential and the charge distribution are coupled through the Poissons equation as well, leading to the Poisson NEGF self-consistency requirement. The 2-D Poisson equation for the cylindrical transistor geometry in Fig. 1 is,

$$\Delta^2 U(r,z) = -\frac{\rho(r,z)}{\varepsilon} \quad (5)$$

Here, ρ (r, z) is the net charge density distribution which includes dopant density as well.

3. Results and Discussions

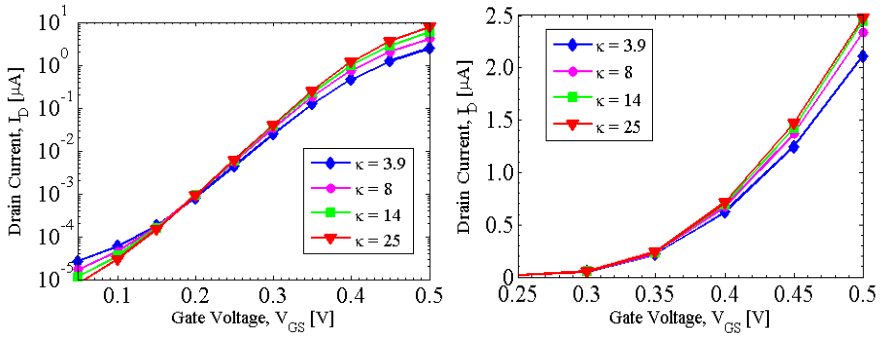
It has been shown that CNTFETs operates essentially ballistic up to several hundred nanometers in length [18]. Since the channel length for CNTFETs of interest is about 10 nm [19], ballistic transport is assumed through the nanotube. We also restrict our attention to steady-state current-voltage characteristics, which are relevant to high-speed operation of digital circuits [20]. For our investigation we selected zigzag CNT as it is semiconducting.

3.1. *Effect of gate insulator dielectric constant*

First we explored the performance analysis by the use of a high-κ coaxial gate insulator. Figs. 2(a) and 2(b) represents the I_D vs. V_{GS} characteristics for both doped contact and SB contact respectively at V_D= 0.5V for four gate insulators, (1) κ = 3.9, (2) κ = 8, (3) κ = 14 (3) κ = 25. Using high-κ gate insulator instead of the SiO_2 gate insulator improves on-current of both Schottky-barrier and doped contact CNT-FET, whereas off current decreases for both cases. But the effect is more prominent in doped contact device than SB contact device. Also the current-voltage characteristics cross for doped CNTFET are at a gate bias of around 0.2V for all gate dielectrics. This is because at that bias ($\approx$ *Eg* /2) the channel potential is approximately in flat band condition with the source fermi level [23]. The scenario can be explained through Figs. 3(a) and 3(b). At the on-state, the charge in the nanotube channel can produce a considerable self-consistent potential which raises the conduction band in the CNT body and increases barrier for electron at source

end. When a high-κ gate insulator is used, the electric field produced by the charge on the tube is effectively screened by the high-κ gate insulator, and the self-consistent potential is smaller. Compared to SiO_2 gate insulator the barrier at the source contact is lower and the conduction band in the CNT body is more effectively lifted down by the gate voltage by applying HfO_2 gate insulator as shown in Fig. 3(a). The barrier at the source contact is lower and the conduction band in the CNT body is more effectively lifted down by the gate voltage by applying HfO_2 gate insulator. Hence it is evident that, High-κ gate insulators afford high capacitance without relying on ultra-small film thickness, thus allowing for efficient charge injection into transistor and meanwhile reducing direct-tunneling leakage currents.

The reason for such behavior in case of Schottky barrier is as follows. Fig. 3(b), which represents the conduction band profiles, for three insulators at the on-state, sheds light on these results. Due to thin gate oxide the Schottky barriers are thin. So the charge density inside the tube is high. When the gate dielectric constant is low, this charge produces a considerable self-consistent potential. As a result the conduction band floats up, which makes the Schottky barrier thicker and the conduction band in the interior of the channel higher. As the tunneling current exponentially depends on the Schottky barrier thickness, the on-current of transistors with low gate dielectric constants is much smaller. Converse is true for high gate dielectric constant oxide materials.



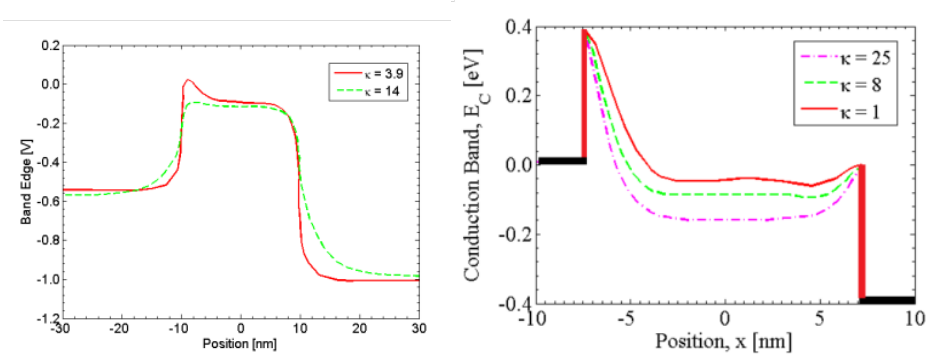
(a) Doped contact (b) SB contact

Fig. 2. The variations of drain current against gate voltage for different values of gate dielectric constant.

3.2. *Effect of oxide thickness*

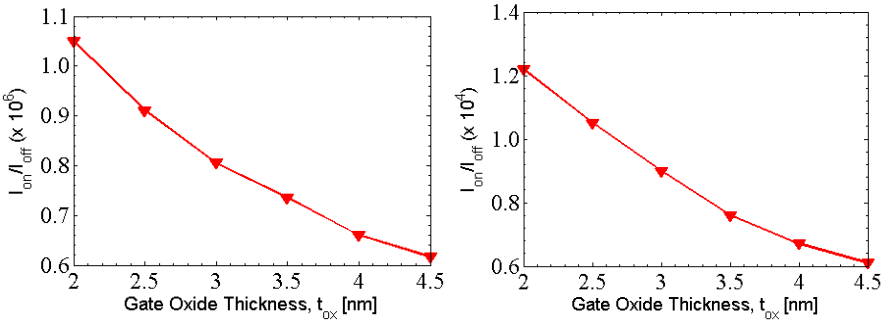
The on/off current ratio for different oxide thickness is shown in Figs. 4(a) and 4(b) for both doped contact and SB contact devices respectively. The on/off current ratio improves with thinner oxide. The on/off current ratio improves from 6.33×10^5 to 1.5×10^6 for the doped contact devices and from 6.1×10^3 to 1.22×10^4 for SB contact devices when the gate oxide thickness changes from 4.5 to 2 nm. The doped contact devices have higher

on/off current ratio and the t_{OX} effects on on/off current ratio is relatively higher in doped contact devices. Shaahin *et al*. also reported on/off ratio for doped contact device with chirality n = 13 is in the order of 10^6 [24]. For thinner oxide thickness total capacitance will increase. So for same gate bias, with thinner oxide the charge in the channel will increase. Consequently conduction band in the channel will be lowered, therefore source to channel barrier will decrease. This is the reason on-current increases with thinner oxide, eventually on/off ratio increases.



(a) Doped contact (b) SB contact

Fig. 3. Conduction band profile at different dielectric constants.



(a) Doped contact (b) SB contact

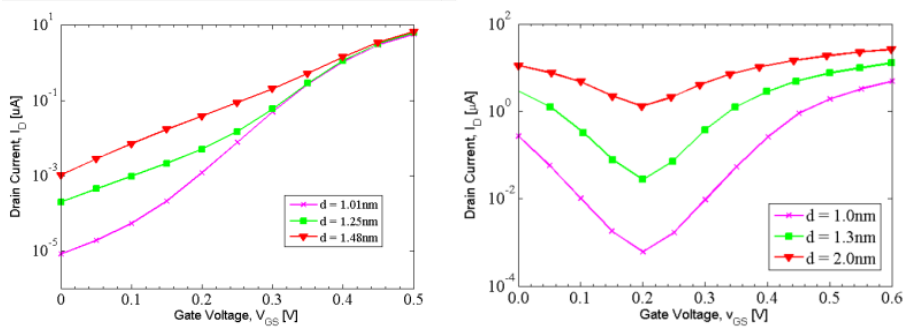
Fig. 4. Variations of on/off ratio against gate oxide thickness, t_{OX}.

3.3. *Effect of diameter*

The impact of diameter on the I-V characteristics of doped CNTFET is investigated in detail. We compared it with the I-V characteristics for SB CNTFET reported by Guo *et al.* [25]. From Figs. 5(a) and 5(b) it is evident that diameter has little effect on the on-current of the device, but with decreasing diameter off-current drastically reduces. Consequently

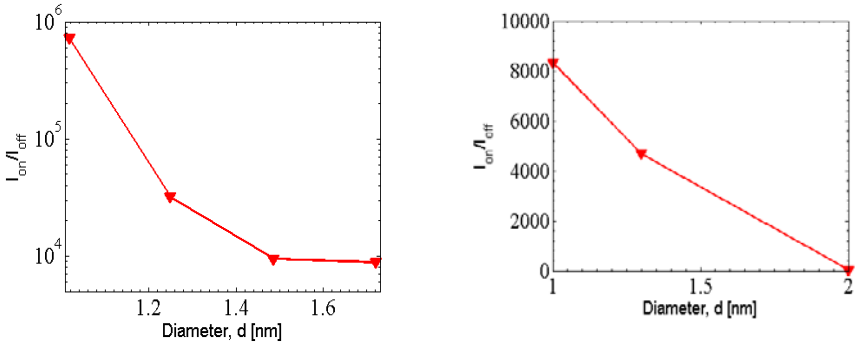
on/off current ratio increases with reduction of diameter which is shown in Figs. 6(a) and 6(b) for doped and SB contact respectively.

There is an inverse relation between channel diameter, i.e., "*n*" value of the channel and its energy bandgap. For higher "*n*" values the valance band edge of channel is closer to the conduction band edge of the source at the low gate bias than lower "*n*" values for doped contact devices [26]. Consequently band to band tunneling leakage current increases in off state. On the other hand in on-state separation between source conduction band and channel valance band is high. As a result there is almost no tunneling in this case and dominant mechanism for electron transport is thermionic emission [26]. For Schottky-barrier contact using a large diameter tube reduces the band gap and significantly increases the minimum leakage current at the ambipolar bias point. At the same time, the on-current is also improved, but the on/off current ratio decreases significantly as the nanotube diameter increases.



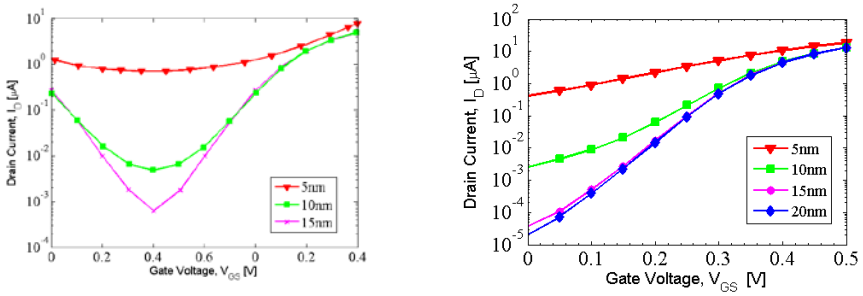
(a) Doped contact (b) SB contact [24]

Fig. 5. Drain current dependence on gate voltage for different diameters.



(a) Doped contact (b) SB contact

Fig. 6. The dependence of on/off ratio on channel diameter.



(a) Doped contact (b) SB contact [25]

Fig. 7. Variations of drain current against gate voltage for different channel lengths.

From Fig. 6 it is evident that the on/off current ratio decreases more rapidly for doped contact device than SB device, with diameter. This is due to the fact that while the on current remains almost same but off current increases more significantly with diameter as depicted.

3.4. *Effect of Channel Length*

Fig. 7 explores the issue of channel length scaling for doped contact and Schottky barrier CNTFET. In order to establish the ultimate scaling limit imposed by source-drain tunneling for CNTFET, very thin gate oxide (t_{OX}= 2nm) is used to ensure excellent gate control electrostatics. We have found that for doped contact device when the channel length is longer than 15 nm, the I-V characteristics are independent of the channel length (as shown in Fig. 7(a)) because the channel is ballistic and effective source to drain barrier is thick and there is no significant tunneling. Scaling the channel length down to10 nm significantly increases the off-current, but the on/off current ratio still exceeds 10^4, which is excellent for digital logic. If the channel length is aggressively scaled down to 5 nm, the on-off current ratio decreases to less than100 due to significant source-drain quantum tunneling. Fig. 8 explains the reason in case of doped contact CNTFETs. It shows conduction band profile for three different channel lengths. We see that when L_{ch} = 30 nm, the effective source to channel barrier is larger. When channel length decreases to L_{ch} = 15 nm, the barrier decreases only slightly. But when L_{ch} = 5 nm barrier decreases significantly, so there is a large amount of tunneling current and off current increases significantly. From Fig. 7(b) it is evident that Schottky barrier CNTFET shows similar I-V characteristics as doped contact but the change in on/off current ratio is less. Figs. 9(a) and 9(b) shows the on/off current ratio for doped and Schottky barrier CNTFET respectively. It is observed that channel length has more significant effect on on/off ratio for doped contact than Schottky barrier contact devices.

In all cases on-off ratio is higher and the effect of scaling is more prominent for doped contact devices than SB contact devices. On-off ratio could be tuned upto 10^6 and 10^4 order of magnitude for doped contact and Schottky barrier contact devices respectively.

Lin *et. al*. demonstrated multiple tube CNTFET with on/off ratios of 5×10^3 up to 5×10^5 and threshold voltage up to approximately 2V [27]. Sangwan *et al*. demonstrated percolating networks of metallic and semiconducting carbon nanotubes FET with mobility up to 50 cm^2/Vs at on/off ratio > 10^3 obtained at channel width W = 50 µm and L > 70 µm for $p = 0.54 - 0.81$CNT s/μm^2 [28]. Sun *et al*. demonstrated carbon nanotube thin film transistors with mobility of 35cm^2 $V^{-1}s^{-1}$ and an on/off ratio of 6×10^6 [29]. Khondaker *et al*. demonstrated semiconducting enriched carbon nanotube align arrays FET with on/off ratio as high as approximately≈ 10^4 at semiconducting enriched (99%) nanotube density approximately ≈ 1-SWNTs/µm [30]. These experimental evidences closely support our analysis.

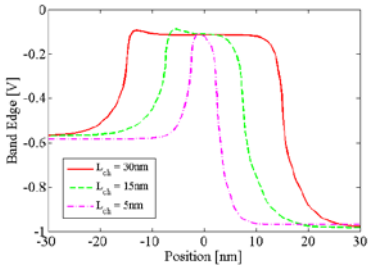
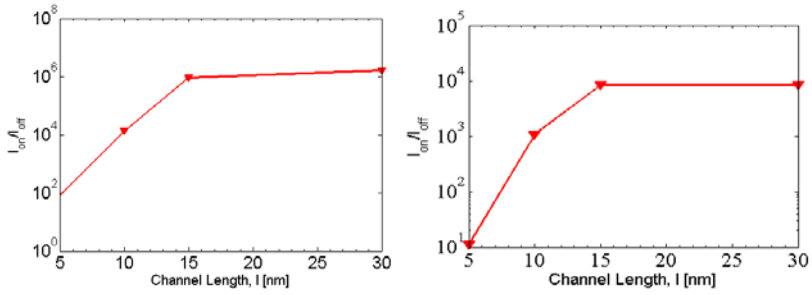


Fig. 8. Conduction band profile for nominal CNTFET at different channel lengths.



(a) Doped contact (b) SB contact

Fig. 9. Variations of on/off ratio against different channel lengths.

4. Conclusion

A study of the effect of different scaling of cylindrical surrounding gate CNT transistors is performed using a π- orbital tight binding model. The impacts of gate dielectric constant, thickness, annotate diameter and channel length are investigated through simulating the behavior of the device depending on these parameters. The result of the simulation study clearly indicates that for optimum configuration of device parameters, the on/off ratio of doped contact device and Scotty barrier device has the potentials to be tuned up to 10^6 and 10^4 order of magnitude respectively. The on-off ratio behavior of doped contact and Schottky barrier CNTFETs for varying device parameters has been summarized in Tables

1 and 2 respectively. The behavioral trends of doped contact and Schottky barrier devices from the tables can be used as a reference to choose optimum configuration of device parameters which being the most important issue to fabricate a high performance CNTFET with good scaling potential.

Table1. Parameter dependent behavior of doped contact CNTFET

Properties	Change	On Current, I_{on}	Off Current, I_{off}	On/off current ratio	Remarks for high performance
Dielectric Constant, κ	Increase	Increases more rapidly	Decreases	Increases more rapidly	High κ dielectric
Oxide Thickness, t_{ox}	Decrease	Increases	Remains almost same	Increases more rapidly	Thinner oxide
Diameter, d	Decrease	Remains almost same	Decreases	Increases more rapidly	Lower diameter Tube
Channel length, L_{ch}	Decrease	Remains almost same	Increases	Decreases	Could be less than 10nm

Table 2. Parameter dependent behavior of Schottky barrier CNTFET

Properties	Change	On Current, I_{on}	Off Current, I_{off}	On/off current ratio	Remarks for high performance
Dielectric Constant, κ	Increase	Increases	No significant decrease	Increases	High κ dielectric
Oxide Thickness, t_{ox}	Decrease	Increase	Remains almost same	Increases	Thinner oxide
Diameter, d	Decrease	Little increase	Decreases	Increases	Lower diameter Tube
Channel length, L_{ch}	Decrease	Remains almost same	Increases	Decreases	Should be larger than 10nm

On-off ratio increases for all the parameter scaling except channel length and the effect of scaling is relatively higher for doped contact devices. However, for a complete evaluation of the performance, effect on transconductance, unity current gain frequency, static and dynamic power dissipation should be studied.

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