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Evaluating DC-DC Buck Converter Efficiency with MOSFET and GaN-FET Technology

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Abstract

This paper assesses the efficiency of DC-DC buck converters utilizing both MOSFET and GaN-FET technology. An analysis is conducted on single-phase switched capacitor buck converter equipped with GaN FETs, highlighting its capability to operate at higher frequencies due to the rapid switching speeds of GaN FETs. This feature results in a decreased size of passive components in comparison to traditional buck converters. Additionally, the specifications for the inductor are also examined. To demonstrate the advantages of GaN FETs over MOSFETs in DC-DC converters, the performance of the GaN-FET based converter is compared with that of a traditional MOSFET-based converter. Key performance metrics evaluated includes output voltage, inductor current ripple, voltage stresses across semiconductor devices, power losses, and overall efficiency. The results indicate that the GaN-FET based converter achieves a lower output voltage at higher duty cycles, reducing losses associated with small duty cycles. Additionally, the proposed converter demonstrates superior performance across all evaluated parameters, reinforcing the efficiency benefits of GaN-FET technology in DC-DC buck converters.

Keywords: DC-DC buck converter; Conduction losses; Switching losses; Voltage stresses; Efficiency.

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1. Introduction

The dc-dc converter finds extensive applications in areas such as voltage regulator modules for microprocessors, battery chargers, and automotive systems [1,2]. The buck converter is widely utilized due to its straightforward design and cost-effectiveness. It achieves an output voltage that is lower than the input voltage by adjusting the duty ratio, which indicates the duration for which the switch remains closed. While the conventional buck converter is relatively easy to implement, it has several drawbacks, including high current ripple and output voltage ripple, which contribute to an increase in the size of the passive components. The increase in the size of passive elements effect efficiency of the converter. To minimize the volume or size of the passive components, it is essential to maintain high

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frequency. The conventional buck converter necessitates a reduced duty cycle for high step-down scenarios, which raises the voltage stress on the semiconductor switches and results in increased losses across these components. This, in turn, affects the overall efficiency of the system.

In order to deal with these various problems, various topologies of buck converter have been presented in literature. A family of converters which enhances the voltage conversion ratio by cascading the exponential switched-cell step down converter [3]. But the converters have the fixed voltage conversion ratio which limits their applications. For attaining wider conversion ratios, increase in the number of diodes has been suggested but it has the effect of increasing conduction losses, cost and also reduction in efficiency of the device [4]. A coupled-inductor based buck converter with an auxiliary circuit to get a high step-down voltage conversion ratio and for reducing the flux linkages and core size has also been introduced in literature [5]. Another approach to attain wider step-down conversion ratio revels use of coupled inductors but the circuit output has pulsating output current and high ripple content [6]. The converters achieve the high step-down conversion ratios by adjusting the turn ratio of the secondary winding but the large leakage inductances could occur because of the high turn ratios associated with the coupled inductor, which can lead to voltage spikes [4-6].

The author has presented the concept of switched capacitor and demonstrated the operation of step-up dc-dc converter [7]. A step-down converter with a very high conversion ratio has been introduced for a non-isolated converter, but the number of active devices needed is more, hence the cost may be increased [8]. A delayed quadratic step-down buck converter with a high-voltage conversion ratio has been introduced but the output voltage stresses on the devices are found to be high [9]. A transformer-less high step-down dc-dc converter with a wider duty cycle range has been found in previous studies [10]. Although, the voltage conversion ratio has improved but the number of active and passive components has increased drastically in this design. A bidirectional dc-dc converter based on switched-cell capacitor has been discussed. Although the converter offers high efficiency but these converters have MOSFET as a switching device [11,12]. The MOSFET has a higher on-state resistance, leading to increased losses, and the operational frequency is also constrained due to elevated parasitic capacitances.

For further improvement in the efficiency of dc-dc converters further, research papers with dc-dc converters using GaN FET switches have also been discussed which indicates that the total power losses can be reduced and efficiency can be increased. GaN-based devices provide several benefits, including increased switching frequencies resulting from their minimal input and output capacitances, along with a decrease in the size of passive components, and decreased switching losses resulting from shorter transition times. They also exhibit lower conduction losses because of their minimal on-state resistance, higher power densities, and smaller die sizes. Furthermore, GaN-based transistors feature reduced on-state resistance, a negative temperature resistance coefficient, and superior electron mobility [13,14]. A dc-dc Zeta converter utilizing GaN E-HEMTs for high step-up applications has also been proposed [15]. This converter demonstrates improved switching

performance, reduced switching losses, lower total power losses, and achieves an efficiency of 97.45 % at a switching frequency of 100 kHz, compared to the 96.18 % efficiency of Si MOSFETs.

Literature also provides analysis of the buck converter utilizing Si MOSFET, SiC MOSFET, and, GaN-based MOSFET [16]. It has been found that SiC and GaN-based FETs have comparatively lower switching losses than Si-based FETs. The overall efficiency of the GaN and SiC-based FETs are also higher when compared with Si MOSFETs. A comparison of the hard switched GaN based boost converter with soft switched Si- based boost converter [17] and advantages of GaN switches for application in Power Electronics has been revealed [18].

Based on these inferences, this paper introduces a DC-DC converter that incorporates a switched capacitor cell and utilizes GaN-FET switches. The converter has been developed by leveraging the latest technologies for optimization and enhancing efficiency. After addressing these aspects, it was found that substituting the switches with GaN-FETs significantly improved overall efficiency. Thus, the primary aim of this paper is to evaluate the performance of the GaN-FET-based converter against a conventional MOSFET-based design. Simulations are employed to assess the performance differences between the proposed and conventional converters. The findings indicate that the GaN-FET-based converter achieves enhanced efficiency across varying output power levels and higher frequencies when compared to the Si-based converter. Additionally, the Si-based converter demonstrates higher conduction and core losses than its GaN counterpart. Section 2 describes the configuration of the proposed converter, while Section 3 examines the comparison based on simulation results, followed by conclusions and discussion in Section 4.

2. Principle of Operation and Design Considerations

The switched capacitor dc-dc converter can step down the voltage at the output for high input voltage. Fig. 1 shows the switched capacitor single-phase dc-dc buck converter with input voltage V_{dc}, the power switches Q_1 and Q_2, a diode D functioning as an uncontrolled switch, identical capacitors C_1 and C_2, two inductors L_1 and L_2, an output capacitor Co, and a load resistance R as shown in Fig. 1. The identical capacitors operate in the first stage which step-down the input voltage while in the second stage it regulates the output voltage. The two switches are given pulses simultaneously. The diode D conducts when the two switches are not in conduction. The two capacitors C_1 and C_2 are charged in series when the switches are not conducting and these capacitors will discharge in parallel through the load when both the switches are conducting. The inductor L_1 is placed in series on input side in order to avoid the sudden change in the current during the transition period of capacitors. For analysis, assuming steady state conditions, the switches and diodes are considered to be ideal. The two identical capacitors are considered with the same capacitance. The output capacitance is assumed to be sufficiently large to keep the output voltage constant. The converter can operate in the two modes depending upon the on-off conditions of the power switches. The two modes of operation are discussed in literature [19]:

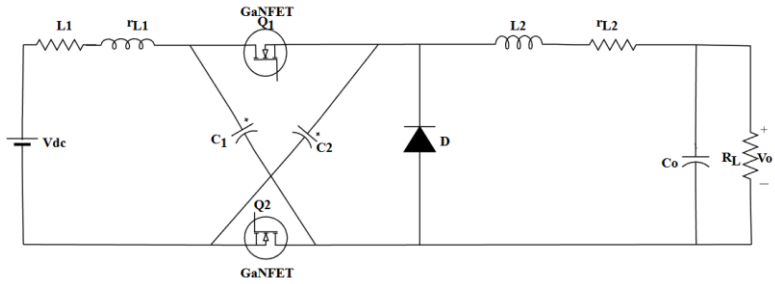

Fig. 1. Proposed converter with GaN FET switches.

MODE 1: Fig. 1(a) shows the operation of the converter in this mode. In this mode of operation, both the switches are conducting. The capacitor C_1 and C_2 are discharging in parallel to the load. The diode is not conducting. The current in the inductor L_2 is increasing in this mode. The voltage across the identical capacitors C_1 and C_2 is assumed to be same that is $V_{C1} = V_{C2} = V_C$. The voltage equations for the proposed converter can be written as:

$$V_{L1} = L_1\left(\frac{dL_1}{dt}\right) = V_{dc} - V_c \quad (1)$$

$$V_{L2} = L_2\left(\frac{dL_2}{dt}\right) = V_c - V_o \quad (2)$$

$$V_O = V_{CO} \quad (3)$$

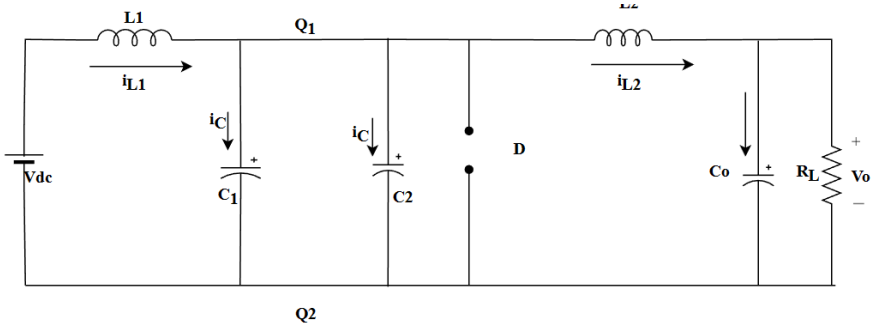

Fig. 1(a). Mode 1 operation of proposed converter.

MODE 2: Fig. 1(b) shows the operation of converter in this mode. During this mode of conduction, the switches are not conducting and both the capacitors are charging in series. The diode D is conducting and the inductor L_2 is discharging to the load. The voltage equations in this mode of operation are given as:

$$V_{L1} = L_1\left(\frac{dL_1}{dt}\right) = V_{dc} - 2V_c \quad (4)$$

$$V_{L2} = L_2\left(\frac{dL_2}{dt}\right) = -V_o \quad (5)$$

$$V_O = V_{CO} \quad (6)$$

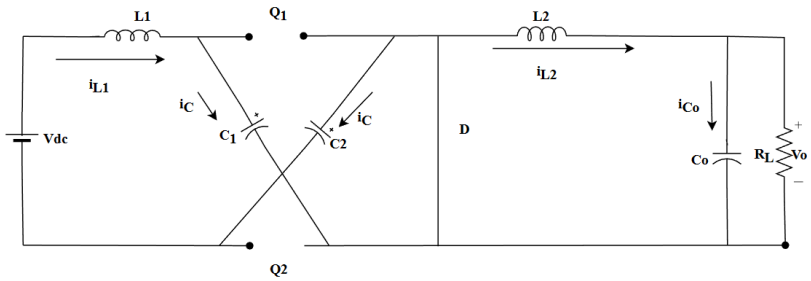

Fig. 1(b). Mode 2 operation of proposed converter

The average value of the inductor voltage over a cycle should be zero for a steady state condition. Therefore, by using the volt-sec balance for the inductor L_1 and L_2 respectively. From Eqs. (1) and (3) of L_1 the expressions (7) and (8) are obtained as follows:

$$(V_{dc} = V_c)D + (V_{dc} - 2V_c)(1 - D) = 0 \quad (7)$$

$$V_{dc} = V_c\,(2 - D) \quad (8)$$

where D is duty cycle given by the ratio of the on period of the switch to the total time period. Similarly for inductor L_2 from Eqs. (2) and (4) the expressions (9) and (10) are obtained as follows:

$$(V_c - V_o)D + (-V_o)(1 - D) = 0 \quad (9)$$

$$V_c\,D = V_o \quad (10)$$

From expression (6) and (8), for steady state operation the dc voltage conversion ratio K can be obtained as:

$$K = \frac{V_o}{V_{dc}} = \frac{D}{2-D} \quad (11)$$

From Eq. 11, we can conclude that the proposed converter will produce the lower output voltage than the conventional buck converter and the voltage conversion ratio is given by $\frac{V_o}{V_{dc}} = D$. Therefore, the proposed converter can thus be used for high step-down applications.

2.1. *Minimum value of inductor*

The ripple current in inductor L_1 and L_2 can be given by the following expressions:

$$\Delta i_{L1} = \frac{(V_o\ (1-D)T_s)}{L_1} \quad (12)$$

$$\Delta i_{L2} = \frac{(V_o\ (1-D)T_s)}{L_2} \quad (13)$$

The minimum values of current through L_1 and L_2 can be given by the following expressions:

$$I_{L1(min)} = I_{L1\,avg} - \frac{\Delta i_{L1}}{2} \quad (14)$$

$$I_{L2(min)} = I_{L2\,avg} - \frac{\Delta i_{L2}}{2} \quad (14\ a)$$

For the continuous conduction, the minimum value of the current should be zero. The average value of the L_1 is equal to the average value of input current whereas the average

value of the current through the L_2 is equal to the load current. Hence, the minimum values of inductor L_1 and L_2 for continuous conduction mode can be given as:

$$L_{1min} = \frac{R(2-D)\,(1-D)T_s}{2D} \quad (15)$$

$$L_{2min} = \frac{R(1-D)T_s}{2} \quad (16)$$

where R is the load resistance, T_s is the switching period and D is the duty cycle.

2.2. *Voltage stress*

Let V_{Q1} and V_{Q2} are the switching voltage stresses of the switches Q_1 and Q_2. Let V_D is the voltage stress across the diode. Therefore, the voltage stresses of the semiconductor switches and diodes respectively can be given by the expression [20]:

$$V_{Q1} = V_{Q2} = V_c = \frac{V_{dc}}{2-D} \quad (17)$$

$$V_D = V_c = \frac{V_{in}}{2-D} \quad (18)$$

The voltage stresses of the proposed converter are less than the conventional buck converter whose voltage stresses are given by $V_Q = V_D = V_{dc}$.

2.3. *Power losses and efficiency*

The average and rms value of the currents through switches during the conduction time can be given by the following expressions respectively:

$$I_{Q1\,avg} = I_{Q2} = I_o D \quad (19)$$

$$I_{Q1\,rms} = I_{rms} = I_o D \quad (20)$$

The average and rms value of the currents through diode during the conduction time can be given by the following expressions respectively:

$$I_{Davg} = I_o(1 - \mathrm{D}) \quad (21$$

$$I_{Drms} = I_o(1 - \mathrm{D}) \quad (22)$$

2.4. *Loss analysis*

The losses have been analyzed considering the parasitic resistances associated with the inductors and semiconductor devices and the capacitors are assumed to be ideal. The switching losses has been neglected for keeping the analysis simple. Let us assume that r_{ds}(on) is the on-state resistance of GaN FET switches. Therefore, the conduction losses of both switches have been determined as under:

$$P_{con} = 2\,r_{ds(on)}.I_o^2.D = 2\,r_{ds(on)}.D.\frac{P_o}{R_L} \quad (23)$$

where P_o is the output power and R_L is the load resistance

The conduction losses in inductor usually occur because of the dc resistance of the winding that forms the inductor. Let r_L is the dc resistance of inductor. Therefore, the conduction loss due to inductor L_2 can be given as [20]:

$$P_{L2} = r_{L2}\,I_o^2 = r_{L2}\,\frac{P_o}{R_L} \quad (24)$$

Similarly, let r_{L1} be the dc resistance of the inductor L_1. Under the ideal condition, the output power should be same as that of input power. Hence, the input current under ideal

condition can be given as $I_{in} = \frac{D}{2-D} I_o$. Therefore, losses due to series resistance of the input inductor L_1 can be given as:

$$P_{L1} = r_{L1} I_{in}^2 = \left(\frac{D}{2-D} \mathrm{Io}\right)^2 r_{L1} \quad (25)$$

Let r_D is the forward resistance of the diode D. Then the conduction losses of diode can be given as:

$$P_{CD} = r_D I_o^2 (1-D) = r_D (1-D) \frac{P_o}{R_L} \quad (26)$$

Let V_F be the forward voltage drop. The power losses associated with the diode can be determined by the expression given under [25]:

$$P_{VF} = V_F I_o (1-D) = (1-D) V_F \frac{P_o}{V_0} \quad (27)$$

The total power losses of the converter can be given as:

$$P_{Total} = P_{con} + P_{L2} + P_{L1} + P_{CD} + P_{VF} \quad (28)$$

The efficiency of the converter can be determined by:

$$\eta = \frac{P_o}{P_o + P_{Total}} \quad (29$$

where P_o is the output power of the converter and P_{Total} is the total power loss.

3. Comparison of Proposed Converter with Conventional Converter

The simulation model for the converter discussed in this work and the buck converter for comparison is designed on parameters presented in Table 1. The specification of the switches has been given in Table 2. The simulation of the converters has been carried out in SIMULINK by considering a duty cycle of 40 % [19]. Using Eqs. (13) and (14), the minimum inductance values for the proposed converter with a selected switching frequency of 500 kHz are determined to be L_{1min} = 14.4 µH and L_{2min} = 3.2 µH.

Table 1. Circuit parameters for simulation of converters using MOSFET and GaN FET.

Parameter	MOSFET	GaN FET
DC Voltage as input (V_{dc})	20V	20V
Inductors	180 µH	75 µH
Series resistances of inductor	0.07 Ω	0.02976 Ω
Output Capacitor, C_o	330 µF	330 µF
Switching Frequency f_s	50 kHz	500 kHz
Load resistor, R_L	5 Ω	5 Ω
Diode resistance, r_D	0.078Ω	0.078Ω
Capacitors $C_1 = C_2 = C$	-	220 µF
Duty ratio	40 %	40 %

Table 2. Specifications of both the power switches for implementation in Simulink.

	Si-MOSFET	GaN E-HEMT
Manufacturer	Infineon	GaN Systems
Part Number	IRFP250NPbF	GS61008P
On-state resistance	0.075 Ω	0.007 Ω

3.1. *Evaluation of output voltage*

The simulation of both the proposed and conventional converter has been conducted using the parameters provided in Tables 1 and 2. Fig. 2 illustrates a comparison of the output voltages of the converter proposed in this study and the conventional converter at a 40 % duty cycle. It has been observed that the final output voltages of the converter presented and conventional converter are observed as 4.6 V and 7.5 V respectively. This demonstrates that the proposed converter can generate a lower output voltage compared to the conventional converter under the same duty cycle.

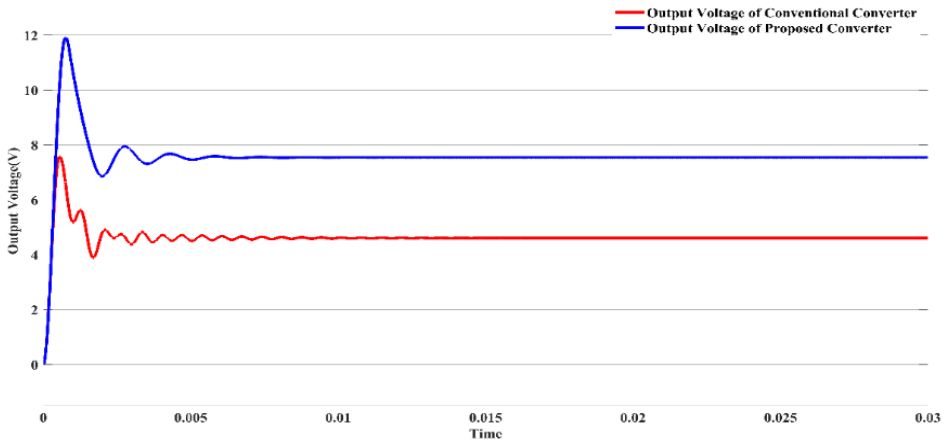

Fig. 2. Comparison of Output Voltages of the converters

3.2. *Evaluation of voltage stress across diodes*

Fig. 3 presents the comparative values of voltage stress for both the converters. The voltage stress appearing across the diodes of the converter discussed in this paper is measured as 12.4 V, while for the conventional converter, the value is observed to be 19.9 V. The results indicate that the diode of the proposed converter experiences lower voltage stress than that of the conventional converter. This allows the use of a diode with a lower voltage rating, which contributes to reducing the overall cost of the converter.

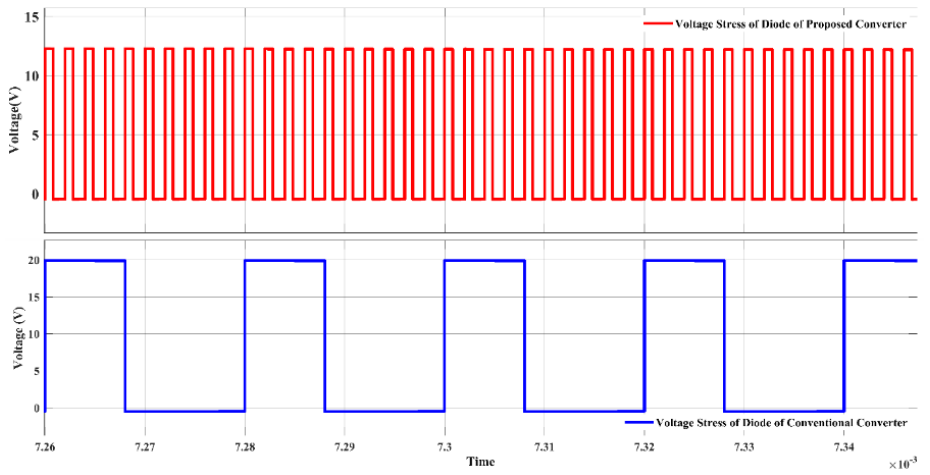

Fig. 3. Comparative Values of Voltage Stress across the Diodes.

3.3. *Evaluation of voltage burden on semiconductor switches*

Fig. 4 gives the comparative values of voltage burden experienced by the GaN FET switches and the MOSFET switches. The results reveal, GaN FET switches have to handle the stress of 12.8V whereas the MOSFET switch of the conventional converter has to handle a voltage stress of 20V. Consequently, a semiconductor switch with a higher rating is required for the conventional converter compared to the GaN FET switch proposed by the author. The increased values of these stresses due to voltage appearing across the switches consistently lead to higher power losses and a reduction in the efficiency of the converter.

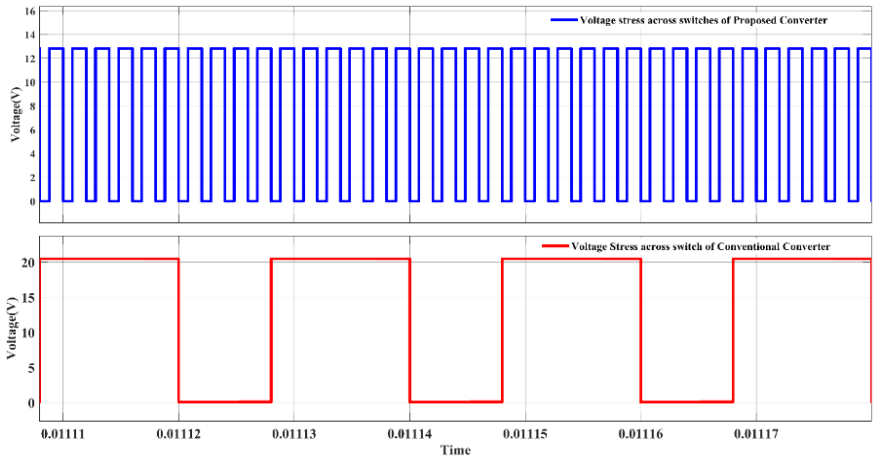

Fig. 4. Comparison of voltage burden across switches.

3.4. *Ripple evaluation of inductor current*

Fig. 5 illustrates the comparison of the ripples in inductor current between the converter proposed here and the conventional converter. The analysis reveals, the value of current ripple for the converter proposed and the conventional converter is approximately 0.083 A and 0.54 A, respectively. Therefore, the ripple in the inductor current of the proposed converter has decreased compared to that of the conventional converter. This reduction in ripple for the proposed converter can lead to lower losses and enhanced efficiency of the converter.

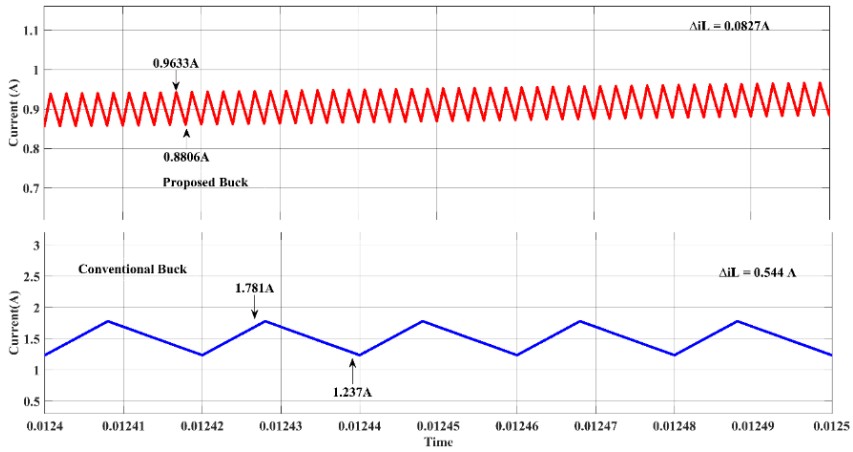

Fig. 5. Comparative ripple evaluation of inductor current in the converters.

3.5. *Analysis of power losses in the converter*

Various power losses occurring in the proposed converter have been computed using the Eq. (28). The calculations of the total losses in the conventional buck converter have been done using relevant equations [19]. It has been assessed that the total losses occurring in the proposed converter are approximately 0.3374 W, while the total losses in the conventional buck converter are about 0.6872 W. Consequently, the overall power losses of the proposed converter are lower compared to those of the conventional converter, which will ultimately result in increased efficiency. The distribution of various losses in the proposed converter is illustrated in Fig. 6.

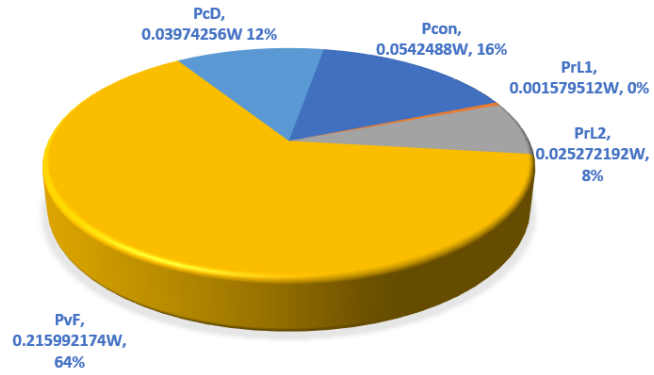

Fig. 6. Distribution of various losses of the proposed converter.

3.6. *Efficiency of converter*

The efficiency of the proposed converter was thoroughly assessed and contrasted with that of a traditional converter by systematically varying the duty cycle from 20% to 70%. At each point within this duty cycle range, detailed measurements were taken for both the input power and output power, which were then used to accurately calculate the efficiency for both converters. The simulated setup ensured that the load conditions remained same for both the conventional and the proposed converters, ensuring a accurate comparison.
Table 3 presents a clear illustration of the efficiency differences between the two converters, revealing the enhanced performance of the proposed design. With increase in duty cycle, the converters need to deliver higher current to the load, and one can observe the performance gap becomes more pronounced at higher values of duty cycle. The proposed converter demonstrates a significantly higher efficiency, particularly in scenarios where the duty cycle is increased to meet greater power demands. This enhanced performance is visually represented in Fig.7 which clearly depicts the superior energy conversion capability of the proposed converter across a broader operational range.

Table 3. Efficiency Metrics for Proposed Converter vs. Conventional Converter

Duty Cycle (%)	Proposed Converter Efficiency (%)	Conventional Converter Efficiency (%)
20	87.3	87.1
30	88.7	88.4
40	90.60	89.6
50	91.6	90.3
60	92.1	91
70	92.4	91.1

Fig. 7 illustrates the efficiency comparison between both the converters across various duty cycle values. At higher duty cycles, the proposed converter maintains significant lead, with an efficiency of 92.4 % at 70 % duty cycle compared to 91.1 % for the conventional

converter. This consistent improvement highlights the superior energy conversion capabilities of the proposed converter, particularly as the duty cycle increases.

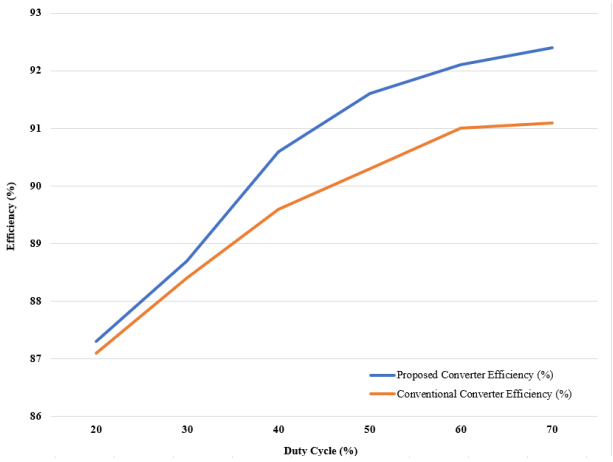

Fig. 7. Efficiency analysis of the proposed converter with conventional converter.

4. Conclusion

A single-phase buck converter utilizing GaN FET switches has been presented in this paper. To evaluate the converter's potential, assessment of the proposed design has been presented against design of the converter based on conventional switches. This comparison focuses on various parameters, including output voltage, voltage stresses, inductor current ripple, power losses, and efficiency. The analysis reveals that the proposed converter can achieve a reduced output voltage compared to the conventional buck converter for same duty cycle, making it suitable for applications requiring greater voltage reduction. Even the voltage stresses across the semiconductor switches and diodes are lower, indicating that switches with less voltage ratings can be easily employed for respective applications. Additionally, the total power losses of the proposed converter are 49 % less compared to the conventional buck converter, resulting in reduced heat dissipation associated with the devices and increased power density. The efficiency performance of the proposed converter is also found to be superior across various duty cycles.

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