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Contact Resistance Induced Variability in Graphene Field Effect Transistors

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Abstract

The success of the graphene field-effect transistor (GFET) is primarily based on solving the problems associated with the growth and transfer of high-quality graphene, the deposition of dielectrics and contact resistance. The contact resistance between graphene and metal electrodes is crucial for the achievement of high-performance graphene devices. This is because process variability is inherent in semiconductor device manufacturing. Two units, even manufactured in the same batch, never show identical characteristics. Therefore, it is imperative that the effect of variability be studied with a view to obtain equivalent performance from similar devices. In this study, we undertake the variability of source and drain contact resistances and their effects on the performance of GFET. For this we have used a simulation method developed by us. The results show that the DC characteristics of GFET are highly dependent on the channel resistance. Also the ambipolar characteristics are strongly affected by the variation of source and drain resistances. We have captured their impact on the output as well as transfer characteristics of a dual gate GFET.

Keywords: Graphene; FET; Simulation; Channel resistance; Contact resistance; Dirac Point.

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1. Introduction

Graphene emerged in 2004 [1] and has attracted enormous interests in the electronic industry for exhibiting a multitude of interesting properties and ultra-fast conductivity exceeding those of conventional semiconductors [2-4]. Specifically, graphene is the first 2-D material, whose unique electronic properties have made it a possible alternative to silicon. The development of graphene field effect transistor has become a part of the quest for the next switch [5-9]. Further, graphene with its planar geometry can be processed with more conventional complementary metal oxide semiconductor (CMOS) technology. According to several studies, the main performance limitation of graphene-based transistors is associated not with the quality of the material, but with external factors that affect the properties of electronic transport. One of the most important spurious elements

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is the contact resistance. Contact resistance is the resistance between the source/drain metal and the graphene channel. Graphene-metal contact resistance is an acute problem for the development of GFET, a high contact resistance (normalized by the width of the contact W), which significantly reduces the apparent mobility of the contacting graphene and prevents its true potential in high-frequency applications [10,11]. This is because the contact resistance is comparable to the resistance of the controlled channel in high-frequency short-channel field effect transistors with graphene (GFET) and therefore, suppresses transductivity and gain [12-14]. However, contact resistance is still poorly understood, although this is a serious obstacle to further improvement. In this article, we developed a simulation method for calculating the current-voltage behavior of graphene-based field effect transistors. At first, the simulation method was validated by experimental results, and then it was used to study the properties of graphene field effect transistors. Contact resistance in FET is vital for digital and analog FET execution. Therefore, we first studied the dependence of the channel resistance on the transfer characteristics and the results are presented in this article.

2. Design Consideration

The cross-section of a graphene FET is shown in Fig. 1. As shown in Fig. 1, a graphene film is sandwiched between the top and back gate dielectrics and is used as a channel between the source and drain electrodes. Ohmic contacts of the source and drain, as well as the top-gate stack, are located on top of the graphene channel.

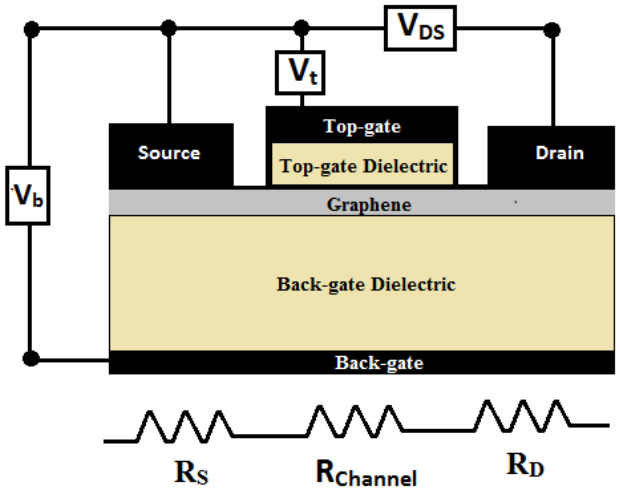

Fig. 1. Schematic diagram of the modelled Graphene Field Effect Transistor (GFET).

In order to test the model, a 285 nm of thick SiO_2 layer is taken, which is grown on a heavily doped Si wafer. The SiO_2 serves as the back-gate dielectric and the Si wafer acts as the back-gate and a 15 nm of hafnium oxide taken as top gate insulator. V_{DS} is the

applied bias between source and drain, while V_b and V_t are the back-gate and top-gate voltages, respectively. In the considered GFET structure shown in Fig. 1, the access region resistances are modelled as a function of the applied gate bias. In GFET, there is no depletion layer because of low thickness of graphene, therefore the working principle is completely based on the ambipolar nature of graphene. The ambipolar field effect can be explained by a 2D metal with a slight overlap of valence and conductance bands. The ambipolarity of graphene allows it possible a graphene transistor to operate with either electrons, holes or both simultaneously. When a positive voltage is applied, the Fermi energy level shifts into the conduction band and as a result the electrons start to populate the conduction band. On the other hand, when a negative voltage is applied, Fermi level drops below Dirac point and holes begin to occupy the valence band. Thus, graphene exhibits dual behaviour in presence of electric field. Graphene differs from semiconductors, because as semimetal graphene requires electrostatic doping instead of impurity doping to conduct electricity. Therefore, the effect of the graphene field is often called self-doping, in which the effect of the electric field makes it possible to control the type of charge carrier and its concentration using an external electric field. Top-gate controls the carrier concentration in the channel. According to electrostatic doping the type of graphene channel changes from n-type to p-type. The back-gate is used to dope the graphene underneath the metal contacts and the ungated graphene. Back-gating provides an additional degree of freedom to control the bias point of the GFET, although the back-gate is an optional feature. The conduction of electrons (holes) in the graphene channel can also be explained with quasi-Fermi levels and the concept of Dirac point, when the drain to source bias is applied. When the gate bias is high, the quasi-Fermi level is above the Dirac point in the channel, and the conduction is due to electrons injected from the source. For holes, the situation is the opposite: when the gate bias is low, the quasi Fermi level is below the Dirac point. GFETs often show quasi-saturation, which is, incomplete saturation. It can be caused by the crossing of the quasi-Fermi level of the Dirac point in the channel. Therefore, the graphene channel does not have a "pinch-off effect" in contrast to the semiconductor channel. Here the source is grounded and the zero-source potential serves as the reference potential in the device. The temperature is taken as 300 K for this study.

3. Simple Modeling Approach

Modeling and simulation are considered two interdependent activities, and these two, as a rule, are an integral part of any device research. Modeling enriches the understanding of the physics of basic devices, while simulation allows us to examine the behavior of a system in a clearly defined way, which often involves many risks in the real world.

In GFET the objective of a simplest modeling approach is to derive an expression for the drain current. In general, the drain current I_{DS} of an FET can be expressed as:

$$I_{DS} = -q\rho_{sh}(x)\, v(x) W \tag{1}$$

where q is the elementary charge, $\rho_{sh}(x)$ and $v(x)$ are respectively the free carrier sheet density and electron velocity in the channel at position x, and W is the channel width transverse to the direction of current flow.

The charge density of a sheet in a graphene channel can be attributed to four different sources [4]:

(i) the intrinsic charge density which can be derived as [15]

$$n_i = p_i = \frac{\pi}{6}\left(\frac{k_B T}{\hbar v_F}\right)^2 \tag{2}$$

(ii) the gate bias dependent sheet charge density expressed as [15,16]

$$n_{GQ} = n_G + n_Q\left[1 - \sqrt{\left(1 + \frac{2n_G}{n_Q}\right)}\right] \tag{3}$$

n_{GQ} where $n_G = \frac{C_{ox}V_G}{q}$ the gate is induced conventional sheet carrier density when the effect of quantum capacitance is neglected, V_G is the gate bias and n_Q is the sheet carrier density due to quantum capacitance, (iii) the charge due to quantum capacitance given by [17].

$$n_Q = \frac{\pi}{2}\left(\frac{C_{ox}\hbar v_F}{q^2}\right)^2 \tag{4}$$

and (iv) the sheet carrier density due to intentional doping which can be determined from the dopant density. The unintentionally doped charge in the absence of any intentional doping is modeled as a fixed charge. The carrier velocity can be modeled as [18,19].

$$v(x) = \frac{\mu\mathcal{E}(x)}{\left[1+\left\{\frac{\mu\mathcal{E}(x)}{v_{sat}}\right\}^m\right]^{1/m}} \tag{5}$$

where, $\mathcal{E}(x)$ is the electric field, μ is the carrier low-field mobility, and v_{sat} is the saturation velocity. The saturation velocity at high carrier density simplifies to [19].

$$v_{sat} = \frac{2}{\pi}\frac{\omega_{op}}{\sqrt{\pi\rho_s}} \tag{6}$$

where, $\hbar\omega_{op}$ is the optical phonon energy. This completes a simplified GFET modeling approach which then can be integrated, with the change of parameters, to obtain a final expression for the drain current I_{DS}. Following the above approach and that due to Thiele *et al.* [5], we have proposed a quasi-analytical model for graphene field effect transistors. The expression for quantum capacitance is given by

$$C_q = \frac{2q^2}{\pi}\frac{k_B T}{(\hbar v_F)^2} ln\left[2\left(1+\cosh\frac{qV_{ch}}{k_B T}\right)\right] \tag{7}$$

where V_{ch} is the potential attached with the quantum capacitance, which may be expressed as:

$$V_{ch} = \left(V_{t-eff} - V\right)\frac{C_t}{C_t + C_b + \frac{1}{2}C_q} + \left(V_{b-eff} - V\right)\frac{C_b}{C_t + C_b + \frac{1}{2}C_q} \tag{8}$$

where C_t and C_b are the top and back gate oxide capacitances respectively and C_q is the quantum capacitance of graphene. Here we are using Matlab as our simulation software.

In order to calculate the value of source drain current we have to determine the sheet carrier density of the system. In our model, the sheet carrier density depends on two factors; the quantum capacitance and the potential associated with the quantum capacitance given in equations (7) and (8). From these two equations, it is clearly seen that C_q depends upon V_{ch} and V_{ch} also depends on C_q. So, these two equations need to be solved self consistently. By using fsolve in Matlab, we are able to solve these two self-consistent equations. The solution provides the values for C_q and V_{ch}. Substituting these determined values in Eq. (10) we finally obtain the value of the drain current.

Applying $E = -dV(x)/dx$, and combining the above expressions for $v(x)$from Eq. (5), v_{sat} from Eq. (6) and integrating the resulting equation, the drain current is obtained as:

$$I_{DS} = -q\rho_{sh}\frac{\mu(-dV/dx)}{1+\frac{\mu(-dV/dx)}{v_{sat}}}W \tag{9}$$

By integrating Eq. (9) within the limits, we get the final expression for the drain current as:

$$I_{DS} = q\mu W\frac{\int_0^{V_{DS}}\rho_{sh}\,dV}{L-\mu\int_0^{V_{DS}}\frac{1}{v_{sat}}dV} \tag{10}$$

As we know contact resistance is the most important parasitic element appearing between graphene and the metal electrodes functioning as the source and the drain. Ohmic contacts to graphene, with low contact resistances, are necessary for injection and extraction of majority charge carriers to prevent transistor parameter fluctuations caused by variations of the contact resistance. However, the metal-graphene contact resistance (R_C) remains the limiting factor for graphene-based electronic devices. To better understand these factors and allow better control of contact technology, a complete physics-based R_C model is an absolute requirement [20-25]. To improve the current understanding, we investigated the issue of carrier transfer between materials of different dimensions. Specifically, we developed a physics-based model in which the first process is responsible for calculating the drain current of the device, then the total resistance (R_T) of the device,

$$R_T = \frac{V_{DS}}{I_{DS}} \tag{11}$$

The second process involves resistance due to a potential step across the junction formed between graphene under the metal and graphene channel (R_{Ch}).

$$R_{Ch} = R_T - (R_S + R_D) \tag{12}$$

where, R_S and R_D are the source and drain contact resistances respectively. The total contact resistance (R_C) is then a combination of the two contributions,

$$R_C = (R_T - R_{Ch}) \quad for \quad R_S \neq R_D \tag{13}$$

$$R_S = \frac{1}{2}(R_T - R_{Ch}) \quad for \quad R_S = R_D \tag{14}$$

Using the residual resistance measurement method eq. 13, a contact resistance (R_C) of 1.4 kΩ can be obtained.

4. Results and Discussion

In order to investigate the effect of contact resistance on the Dirac point and the I~V characteristic of GFET, we have considered a GFET structures with a channel length of 1 μm and a width of 2.1 μm. For this study, we took various contact resistances from 500 ohms to 1500 ohms. The other material parameters for the simulation are listed in Table 1 [5].

Table 1. Other GFET parameters used through this work.

Parameters	Value	Parameters	Value
t_t	15 nm	V_{t0}	1.45 V
t_b	285 nm	V_{b0}	2.7 V
ϵ_t	16	μ	300 cm^2/Vs
ϵ_b	3.9	V_b	-40 V
v_F	$10^6\ m/s$	$\hbar\omega_{op}$	55 meV

To begin with, the transfer characteristics of the considered dual gated GFET are calculated. The plots are presented in Fig. 2(a) at $V_t = -1V$, $V_{DS} = -1V$ and $V_b = -40\,V$. In Fig. 2(a), the current value decreases with increasing drain resistance (R_D), which is very obvious in the overall structure of the field effect transistor. In fact, this observation provided sufficient opportunities for calculating the $I{\sim}V$ characteristics of the GFET by adapting the source and drain resistances. In addition, in Fig. 2(a), it is observed that the Dirac point gradually shifts to the left with increasing drain resistance value (R_D) at constant source resistance(R_s). However, the scenario becomes opposite in Fig. 2(b) when the drain resistance (R_D) becomes constant and the value of the source resistance (R_s) increases. The curves, as well as the Dirac points, are now shifted to the right with increasing source resistance (R_s); the rise in the current scale, however, is maintained.

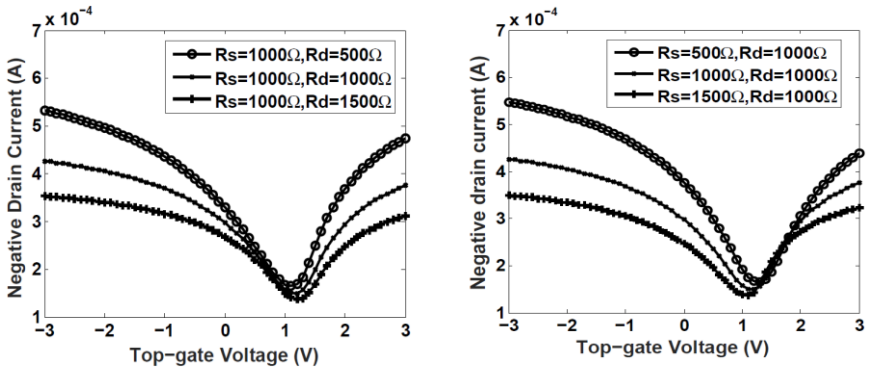

Fig. 2. (a) Transfer characteristics of constant source GFETs with different drain resistances, (b) transfer characteristics of constant drain resistance GFETs with different source resistances.

This is a clear manifestation of the ambipolar nature of graphene, which, in turn, resembles the fact that ambipolar characteristics can be suitably developed by tailoring the contact resistance. Here, electrons predominate on the curves to the left of the Dirac points, and holes on the right dominate with a continuous change in the charge of the carrier over the entire curve. We also noticed that the curves left to the Dirac point intersect at a point showing the same current at a point with constant source resistance (R_S), while with a constant drain resistance (R_D), the curves intersect each other right to the Dirac point. Although the transfer characteristics (the dependence of the gate voltage V_t on the drain current identifier) of graphene field effect transistors typically display a V-shaped curve, several reports show abnormally distorted transfer characteristics [26]. Such a distortion observed in our result, which indicates that, at a high value of R_S and R_D, the characteristics of the $I{\sim}V$ transport curve are deformed compared to its V-shape. As a result, the field effect mobility decreases, and therefore it is technologically important to determine the origin of the distortion. This tendency towards displacement of the Dirac points shows that the Dirac points are very strongly influenced by the change in the source and drain resistances. The exponential convergence of all the inflexion points of the GFET with different source and drain resistances is of interest. The output characteristics of the GFET are investigated for various combinations of source and drain resistance, and the results are presented in Figs. 3(a) and 3(b). Fig. 3(a) shows that the drain current increases with decreasing resistance, as expected. The output characteristics shown in Fig. 3(a) have basically three features. First, the curves have linear regions for low negative drain-to-source voltage, with a tendency to very weak saturation with increasing V_{DS} magnitude. Secondly, the kink feature is also noticeable. But this characteristic is observed only in limited cases, for example, kink effect is noticed with a low drain resistance of 500 Ω. Finally, all the curves tend to touch at a point resulting in zero or negative trans-conductance.

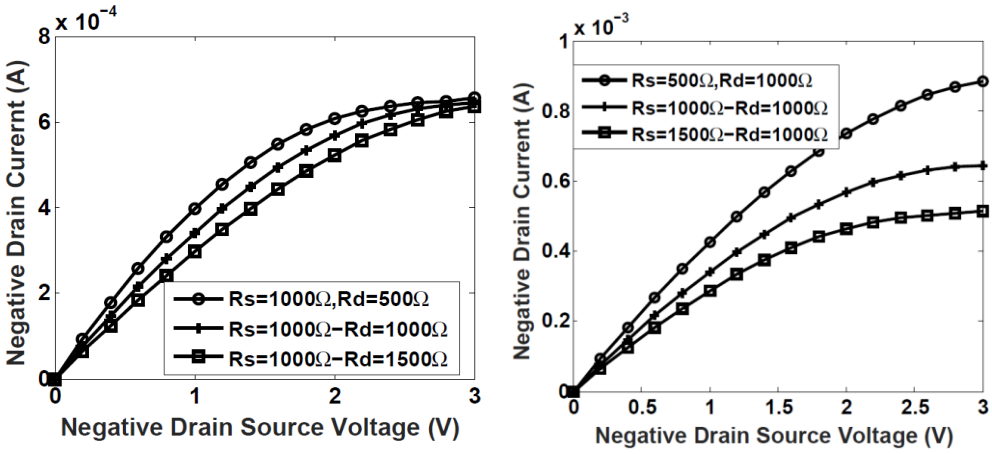

Fig. 3. (a) Output characteristics of constant source GFETs with different drain resistances, (b) output characteristics of constant drain resistance GFETs with different source resistances.

With a constant source resistance, the effect of a change in drain resistance on the drain current is minimal, but the drain current decreases with a sufficient change in value, indicating that the effect of the source resistance on the output characteristics is stronger than that of the drain resistance. Fig. 4(a) and (b) show the calculated output and transfer characteristics of the simulated GFET. In both cases, the source and drain resistances are taken the same. The simulation results show that with an increase in resistance, the drain current decreases, as it has already happened in previous cases. In the discussion above, we saw that in Fig. 4(a) the curves will never enter the ambipolar region only by increasing the negative V_{DS} value. Indeed, in a purely p-type channel, the points of charge neutrality at zero drain bias are above the level of the quasi-Fermi hole for each point of the channel. As V_{DS} increases, the charge neutrality point on the drain side channel increases with minimal impact on that of the source side. In such a situation, the I_{DS}~V_{DS} curves do not show kink characteristics and the curves are in the linear and saturation regions. Now coming to Fig. 4(b), we observed the same result in the transfer characteristics as seen in Fig. 2(b). When we change the resistance of the source and drain in the same ratio, the Dirac point shifts to the left. These characteristics of the curves clearly enhance the ambipolar nature of graphene, which will allow engineers to modify charge carriers accordingly by adjusting the ratio of source and drain resistances. In addition to examining the current-voltage characteristics of the GNRFET with the variation of ratio of R_S and R_D, the channel resistance value of the GFET is also vital.

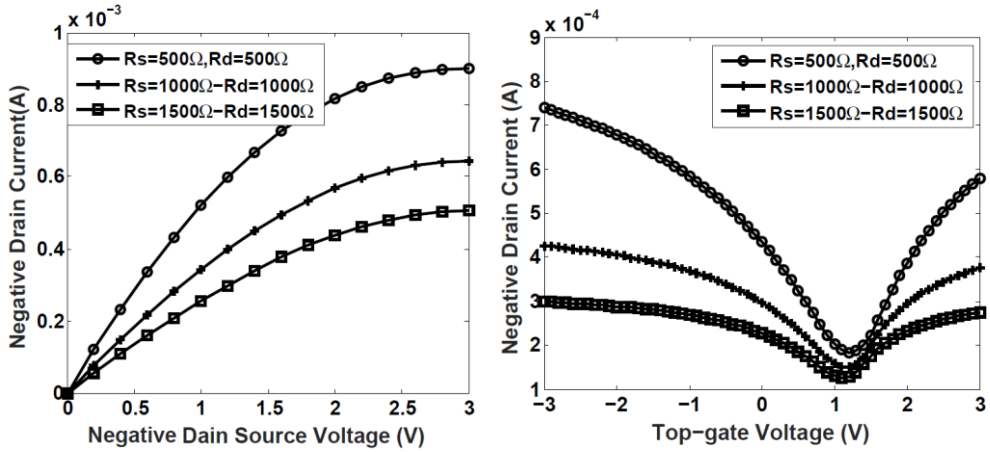

Fig. 4. (a) Output characteristics of GFETs with equal source and drain resistances, (b) transfer characteristics of GFETs with three different combinations of equal source and drain resistances.

The channel resistance computed from the output characteristics is plotted in Fig. 5(a) for three different values of V_t. It is observed that the channel resistance is a swiftly decreasing function of the drain source voltage. In addition, it is worth mentioning that the rate of decrease in the channel resistance is noticeably reduced with increase in negative

value of the top gate voltage. The channel resistance determined from the transfer characteristic is depicted in Fig. 5(b). It is interesting to notice the Gaussian-like peaks exhibited by the channel resistance. The peaks are not only enhanced in their values but also in their locations (in the V_t scale) when negative V_{DS} is reduced. Further, there exists a strong correlation between V_{DS} and V_t corresponding to the peaks. From the available data it is observed that $|V_{DS}| + V_t = 2$ V for each peak. Thus, to sum up, the channel resistance can be controlled by the drain-source voltage and the top-gate voltage individually or jointly.

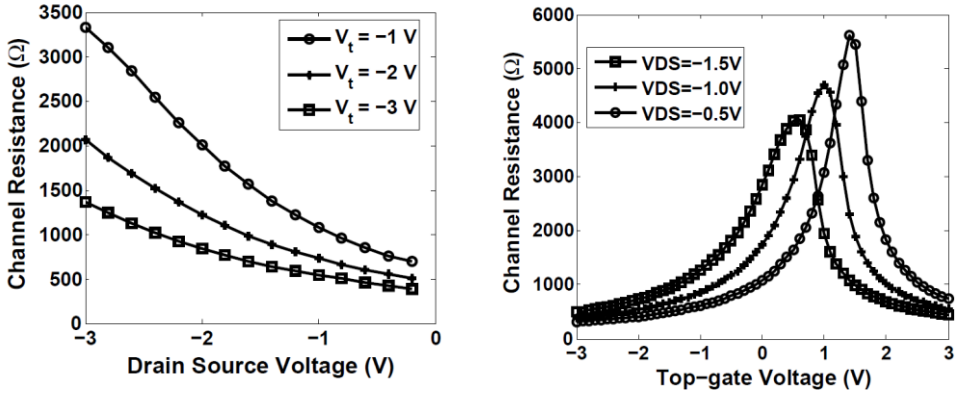

Fig. 5. (a) Channel resistance GFETs as for three different gate voltages, (b) channel resistance of GFETs for three different drain-source voltages.

4. Conclusion

The process variability always affects the device parameters which in turn influences the device characteristics. The variability of source and drain contact resistances and the consequential effects are discussed in this work using a simulation method developed by us. The contact resistance affects the Dirac point of the transfer characteristics by shifting it in the V_t scale; interestingly, the source and drain contact resistances produce shifts in opposite directions. The source contact resistance influences the output characteristics more strongly than the drain contact resistance. The channel resistance is also affected by the contact resistances which in turn modulates the device parameters. A plot of the channel resistance against the top gate voltage, which exhibits Gaussian-type curves, witnesses a systematic shift in the peak when the drain to source voltage is varied. Finally, one can opine that the study of contact resistance variability is very important to optimise the performance of GFETs.

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